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Analysis of Strategies for Improving the Performance of SiC Semiconductor Devices

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Abstract. Due to its wide bandgap, high thermal conductivity, and high-temperature, high-frequency, and high-power characteristics, silicon carbide (SiC) has been widely applied, especially in the field of electric vehicles, power conversion and photovoltaic inverters. However, there are still some defects in the utilization of SiC-based semiconductor devices, such as lattice mismatch, material defects, and interface defects. Enhancing the stability and reliability of SiC devices themselves is an urgent issue to be solved in order to improve their performance. This study proposes four strategies to enhance the performance of SiC semiconductor devices, with a focus on improving material quality, optimizing device structure, and addressing thermal management challenges. These strategies have made significant progress in the reliability and efficiency of silicon carbide devices, especially for high-power, high-frequency applications such as electric vehicles and photovoltaic systems. Moreover, a liquid-cooled heat sink design based on topology optimization is adopted to improve the heat dissipation efficiency. Benefiting from its wide bandgap (3.26eV), high thermal conductivity (~4.9 $W\cdot cm^{-1}\cdot K^{-1}$), and strong breakdown field (~3MV/cm), SiC is inherently suited for high-temperature, high-frequency, and high-power operation. The strategies proposed in this study further leverage these advantages to enhance device performance and reliability.

Keywords: PVT; MOS Structure; Inverted Trigger Electrode; Photoconductive Semiconductor Switch; SiC.

1. Introduction

Silicon carbide (SiC), as a wide bandgap semiconductor, features a wide bandgap (approximately 3.26 eV) and high thermal conductivity, making it suitable for applications in high-temperature, high-frequency, and high-power scenarios. Compared to Si, SiC can operate at higher voltages, withstand greater current densities, and maintain better reliability even at higher temperatures, thus being widely used in high-end applications such as electric vehicles, power conversion systems, and solar inverters [1].

However, there are still significant challenges in the performance control of SiC, mainly including lattice mismatch and material defects. There is approximately a 19% lattice mismatch between Si and SiC, which leads to many defects such as dislocations and cracks during the growth of SiC films. Obtaining high-quality SiC films on silicon substrates and further improving the electronic properties of SiC materials are currently research hotspots [2]. Interface defects in SiC devices, especially in SiC MOSFETs, can reduce carrier mobility and the stability of the threshold voltage. To address this issue, the regulation of SiC materials and the improvement of device stability are among the future development directions of SiC.

The polytypes of SiC (such as 3C, 2H, 4H, and 6H) have significant differences in crystal structure, band structure, and carrier mobility. 3C-SiC and 2H-SiC typically have lower carrier mobility and are thus used in some low-power applications. In contrast, 4H-SiC and 6H-SiC have larger bandgaps and higher carrier mobility, making them widely used in high-power electronic devices. Research indicates that 4H-SiC has high thermal stability and electrical performance, thus having broad prospects in high-temperature and high-pressure applications [3]. Despite this, the differences in thermodynamic stability and electronic properties among different polytypes remain an important research direction.

The quality of SiC films determines the performance of devices. Due to the lattice mismatch between Si and SiC, SiC films grown on Si substrates often have defects such as dislocations and cracks [2]. Current research mainly focuses on improving the growth of SiC films through techniques such as chemical vapor deposition (CVD), solid-phase epitaxial growth, and nitridation. Nitridation treatment of SiC films can effectively reduce defects in SiC films and improve their crystal quality and electronic properties. The quality of SiC films has significantly improved, providing better conditions for applications in high-frequency and high-power scenarios.

Due to the presence of defects at the SiO2/SiC interface in SiC MOSFETs, the carrier mobility is relatively low, which limits the performance of the devices [4]. Methods such as NO annealing, nitridation, and metal doping have been used to improve the interface quality of SiC MOSFETs and increase their carrier mobility. In addition to the above aspects, SiC devices may experience threshold voltage drift caused by Bias Temperature Instability (BTI), a phenomenon in which prolonged electrical bias and elevated temperature lead to gradual threshold voltage shifts. This degradation mechanism shortens the device's lifespan and reduces its stability and reliability [4]. To solve these problems, improvements have been made to the performance of devices through methods such as annealing optimization and different metal doping. SiC semiconductor devices still face technical challenges such as packaging design issues, electromagnetic interference problems, and short-circuit protection problems during application. This study will discuss four strategies to enhance the application performance of SiC semiconductor devices, including adopting different growth processes (such as PVT method and introducing in-situ strain); improving interface states through structural means (MOS structure design); and making overall structural adjustments (new material systems). The application performance and device improvement mechanisms of each strategy will also be analyzed. Through these four different methods, the stability of the devices has been enhanced, and SiC has been optimized to varying degrees, enabling it to play a greater role and advantage in various fields.

2. Strategies for Enhancing SiC Semiconductor Devices

2.1. Design metal-oxide-semiconductor composite structures

Semiconductor neutron detectors predominantly utilize silicon-based devices, primarily those employing the Schottky barrier diode (SBD) structure. However, these devices exhibit significant limitations, including high leakage current and poor energy resolution. Excessive leakage current severely compromises operational stability and accuracy, amplifies signal noise, and reduces detection precision. Inadequate energy resolution impedes the detector's ability to distinguish various neutron reaction channels, thereby limiting its high-precision functionality. To address these challenges, a metal-oxide-semiconductor (MOS) structure-based design has been developed. By optimizing the thickness of the oxide layer and neutron conversion material, the detection capability is substantially enhanced. Comparative analysis of detector performance under varying oxide layer thicknesses reveals that a 60 nm oxide layer effectively reduces leakage current while maintaining favorable energy resolution (Figure 1). Experimental data conclusively demonstrate that leakage current decreases progressively with increasing oxide thickness, albeit at the expense of energy resolution. This trade-off arises because excessive oxide thickness induces non-uniform charge accumulation and electric field distribution, adversely affecting response speed and resolution. The 60 nm oxide thickness is empirically validated as the optimal configuration, achieving an ideal balance between leakage current suppression and energy resolution preservation, thereby enhancing overall detector performance. Validation experiments employing a D-T neutron source confirm that the optimized detector successfully discriminates between different neutron reaction channels. The detector demonstrates exceptional detection capabilities, particularly in resolving thermal neutron reaction pathways with high resolution. Simulation results are in close agreement with experimental data [5]. The use of 4H-SiC as the semiconductor substrate ensures remarkable stability under high-temperature and high-radiation conditions, making it particularly suitable for extreme environments. Leveraging the wide bandgap advantage of 4H-SiC, the detector maintains low leakage current and high detection efficiency even under intense radiation and elevated temperatures. Through comprehensive optimization of each component, the proposed design effectively mitigates the drawbacks of conventional detectors, significantly improving precision, stability, and environmental adaptability. This approach provides a novel methodology for the development of high-precision neutron detectors.

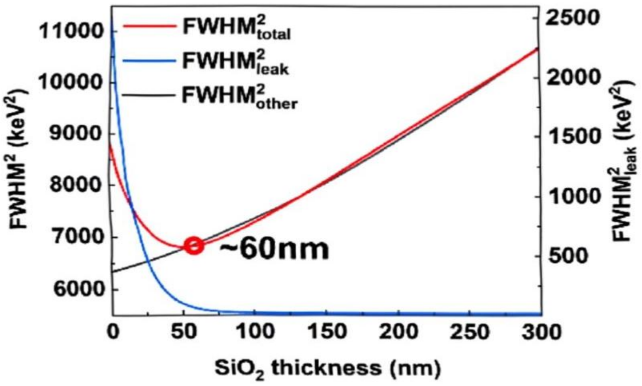


Figure 1. The influence of oxide thickness on the performance of semiconductor devices [5]

2.2. Optimization of SiC synthesis methods

2.2.1. Physical vapor transport (PVT) method.

The SiC focusing ring fabricated by physical vapor transport (PVT) method was studied to enhance the etching resistance of semiconductor reactive ion etching (RIE). The structure has excellent etching resistance and plays a good role in uniformly diffusing the plasma across the entire etching area, effectively avoiding damage to other parts. The SiC focusing ring prepared by the traditional CVD method is prone to being etched away after long-term use and has poor etching resistance. Therefore, it is necessary to improve the material of the focusing ring to extend its service life and etching resistance. Research shows that the SiC focusing ring synthesized by the PVT method has larger grains (about 2000μm), while the SiC focusing ring synthesized by the traditional CVD method has smaller grains (about 10μm). The larger the grains, the fewer the grain boundaries, and the grain boundaries are relatively fragile parts that are more easily etched away. Therefore, the surface of the PVT SiC focusing ring changes little after etching treatment, but the surface of the CVD SiC focusing ring has many sub-micron-sized hole defects, and these holes are mainly distributed at the grain boundaries, further indicating that the grain boundaries are very vulnerable to damage during etching (Figure 2). The etching rate of the PVT SiC focusing ring is only 0.03μm/min, much lower than that of the CVD method at 0.09μm/min, indicating that PVT SiC has good corrosion resistance and a longer service life [6]. Based on the above analysis results, it can be known that the large-grain SiC focusing ring fabricated by the PVT method can significantly improve its etching resistance, extend its service life, and reduce particle contamination during etching. It can be used in the selection of materials and process improvement for RIE equipment in semiconductor manufacturing, and has great significance and broad application prospects in future research.

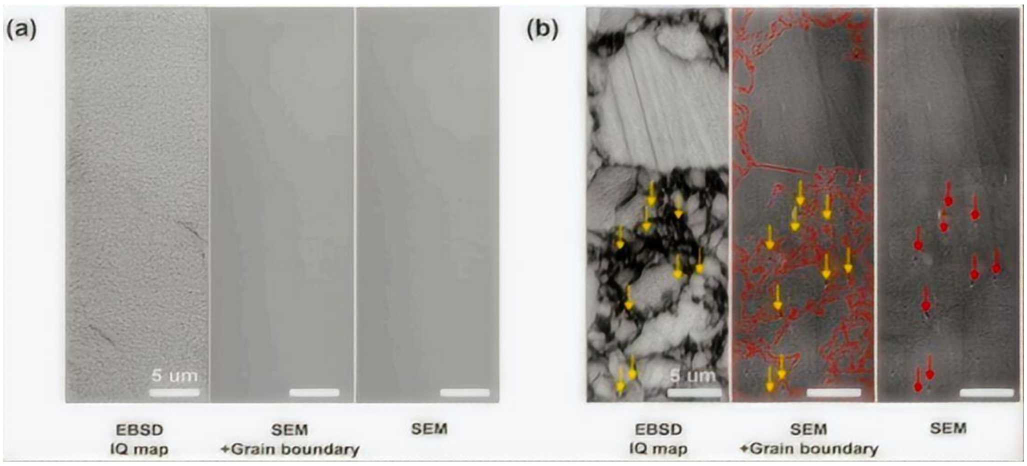


Figure 2. The surface comparison of PVT SiC and CVD SiC after RIE treatment [6]

In the current RIE process of semiconductor manufacturing, it is required to transfer the pattern to the topmost layer, such as copper, other metal compounds or silicon. As an important component of the RIE process, the focus ring is used to fix the entire wafer sample, ensure the distribution of plasma, and completely remove the wafer center within a certain thickness range for etching. However, the focus ring is prone to severe etching when exposed to plasma and reactive gases for a long time, resulting in a rough surface, a large number of particles, surface defects, and a reduced remaining amount. These problems are particularly prominent in SiC focus rings prepared by traditional CVD methods with a diameter of 12 inches, a grain size of only about 10μm, and many grain boundaries. This is because it is prone to cause hole defects at the grain boundaries, leading to continuous degradation.

In response to the above problems, the manufacturing process is beginning to favor the use of PVT for production. PVT is a method of directly sublimating and depositing raw materials at high temperatures to obtain SiC crystals. Compared with the small-grained (about 10μm) and grain-boundary-rich SiC focus rings produced by the traditional CVD method, the PVT structure has more advantages, namely larger grains (about 2000μm) and fewer grain boundaries. The reduction in the number of grain boundaries reduces the invasion channels for plasma etching and fundamentally avoids the occurrence of hole defects. The etching rate of PVT SiC is 0.03μm/min, which is only 1/3 of that of CVD SiC (0.09μm/min), demonstrating its better etching resistance. After etching, the surface roughness is significantly reduced, with PVT SiC being about 0.71μm and CVD SiC reaching 3.64μm. Due to the difference in surface roughness, it leads to different results in the stability of plasma distribution and etching uniformity. In addition, the current ripple of the drive system also has a significant impact on the stable distribution of plasma and the etching effect on the focus ring surface. To more effectively control the stability of current output, a four-phase interleaved parallel Buck drive structure as shown in Figure 3 is adopted in this paper to achieve low ripple and high-frequency current drive. This structure can significantly reduce the current ripple from 2.5 A to 0.2 A, thereby further improving the etching resistance and etching uniformity of the focus ring. In actual semiconductor manufacturing, the improvement in etching resistance can not only increase the lifespan of components but also avoid particle contamination on the wafer surface, thereby improving yield and equipment utilization rate [7]. Large-grained SiC focus rings can reduce the downtime and calibration time required for component replacement, which is beneficial to increasing the production line speed. For more advanced processes, the fewer surface defects there are, the easier it is to achieve uniform etching effects. Overall, large-grained PVT SiC can achieve relatively excellent mechanical strength, etching resistance, and surface stability. Its use in RIE equipment also ensures the high stability of the material in the later stage. Combined with the optimized low-ripple current drive system design, it provides an important reference for the future collaborative optimization of semiconductor manufacturing equipment materials and circuit structures.

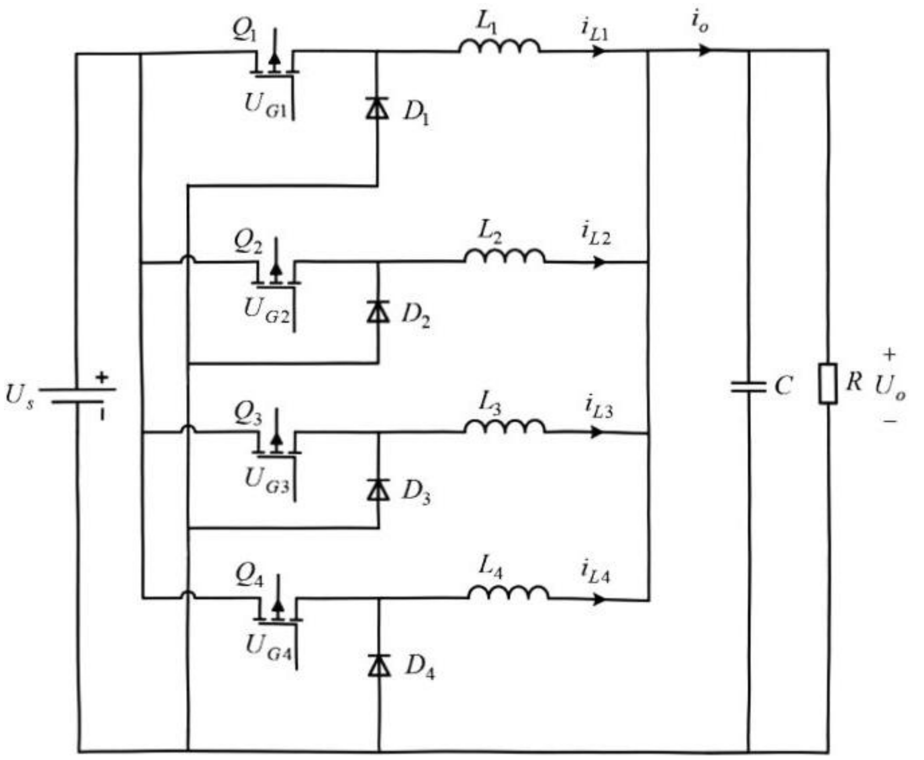


Figure 3. The four-phase interleaved parallel Buck converter topology for driving semiconductor lasers [7]

2.2.2. In-situ growth regulation.

One of the main difficulties in using 3C-SiC semiconductor materials for high-performance microelectronic devices is the difficulty in controlling strain during the growth process. Due to the lattice mismatch between 3C-SiC and the Si substrate, the residual strain generated during the epitaxial growth process will cause defects in the epitaxial film and lead to phenomena such as wafer bending, uneven wafer thickness, and decreased pattern accuracy, ultimately resulting in unstable performance of the device. For MEMS, it inherently requires a certain rigid structure and has very strict requirements for the mechanical properties of the device. As shown in Figure 4, the strain state under different C/Si ratios can significantly change the bending degree of the cantilever beam in the microstructure of the 3C-SiC film. The change from tensile to compressive strain reflects the strain response of the device structure integrity. If the strain is too large during epitaxial growth, it will cause physical bending or uneven fractures in the device, further destroying the original accuracy and reliability of the device. To overcome this problem, the C/Si ratio can be controlled during the growth process to obtain the desired strain within a wide range. The C/Si ratio can be adjusted during growth to change the strain state of the epitaxial film. A film with positive strain can be obtained under carbon-rich conditions, and a film with negative strain can be obtained under silicon-rich conditions. By appropriately adjusting the C/Si ratio during the growth process, a process from tensile strain to compressive strain or even zero strain can be achieved on the film. The corresponding structural effects of this adjustment have been verified in the cantilever device shown in the SEM in Figure 4. This adjustment method does not require additional film thickness, doping, or other subsequent treatments, making it convenient for industrial production.

Of course, from the perspective of process control, in addition to effectively reducing wafer bending, it can also improve the crystalline quality of the film. By changing the C/Si ratio, the best crystal structure can be obtained when the film is in different strain states, thereby reducing defect density and improving the electrical and mechanical properties of the device. The 3C-SiC film optimized on MEMS devices has good mechanical stability, and the internal stress of the film layer is close to zero. As shown in the strain control in Figure 4, when the C/Si ratio is 1.125 to 1.165, the film is almost not bent, which is a key window interval for achieving high-performance devices. It can make the size of sensors or actuators with high response accuracy and high sensitivity larger under the same conditions. By controlling the film thickness, a good thickness control effect can be achieved while controlling the strain. The larger the C/Si ratio, the thinner the film thickness, but the higher the crystal quality. A high crystalline quality can still be obtained under the premise of a small film thickness and a short growth time. This is very beneficial for large-scale production. One reason is that it reduces production costs, and another reason is that it simplifies microprocessing and improves the production rate of MEMS devices. In summary, adjusting the strain state of 3C-SiC films by regulating the C/Si ratio compensates for the disadvantages of traditional strain control methods in improving film quality and device performance. It also overcomes the drawbacks of thick film growth, ensuring the mechanical and electrical properties of the film and laying the foundation for the further development of MEMS devices [8].

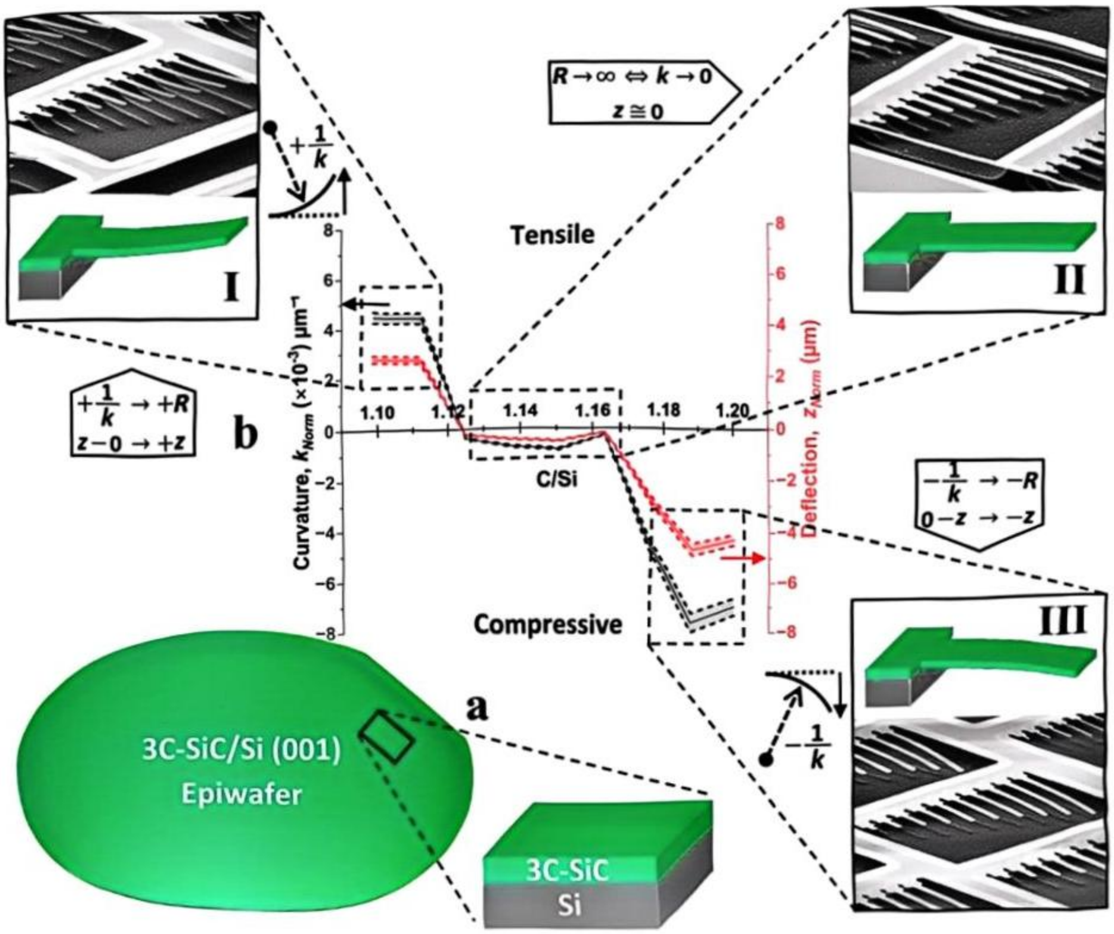


Figure 4. The influence of C/Si ratio on the strain state of 3C-SiC/Si epitaxial layer and the morphology of devices [8]

2.3. Theoretical simulation optimization

How to balance cost, efficiency and reliability in a three-level photovoltaic inverter has become the core issue. Traditional Si NPC inverters have low costs but cannot achieve high efficiency. All-SiC NPC inverters can ensure efficiency but have high device costs, which is not conducive to promotion. However, a Si/SiC H-ANPC hybrid inverter composed of Si IGBTs and SiC MOSFETs can improve efficiency while reducing the cost burden of devices. Due to the fact that a small number of SiC MOSFETs bear almost all the high-frequency switching losses, they are subjected to excessive thermal stress during long-term operation, which becomes one of the main factors affecting the lifespan of the entire system. The research first conducted accelerated electrothermal power cycling tests on Si IGBTs and SiC MOSFETs respectively, and used multiple models to perform equivalent thermal simulation on the device, establishing and verifying their fatigue degradation models. Then, the failure probability distribution of the devices under actual application conditions was calculated using the Monte Carlo method based on the photovoltaic mission profiles in different regions, rather than relying on external test data for modeling as previously done to obtain the expected lifespan values to reduce errors [9]. In the Si/SiC H-ANPC, the degradation rate of SiC MOSFETs due to long-term high-temperature operation and frequent switching is much faster than that of Si IGBTs. The impact of three different heat dissipation configurations on the temperature distribution clearly indicates the key role of optimizing heat dissipation design in extending the lifespan of SiC MOSFETs. Supplementary heat pipes are used to reduce the junction temperature. Compared to the situation where there is only a single heat sink without supplementary heat pipes, even if the SiC MOSFET is still in the high-temperature area, when they are separately installed on different heat sinks and the fan position is changed to increase the airflow to the SiC MOSFET, the junction temperature can be reduced by 3°C, significantly extending the device lifespan without any additional cost. The prediction results show that in Seattle, the B10 lifespan of the optimized SiC MOSFET can reach 31.4 years, which is still some distance from the all-SiC NPC inverter. In the high-temperature environment of Arizona, it can still maintain approximately 22.8 years. The heat dissipation optimization effect indicates that this design can effectively improve the reliability of SiC MOSFETs in the Si/SiC H-ANPC inverter. Through accelerated life testing and modeling of SiC MOSFETs in Si/SiC hybrid inverters, combined with reliability assessment analysis and optimized heat management, the lifespan bottleneck caused by excessive junction temperature of SiC MOSFETs due to high-frequency switching losses in Si/SiC hybrid photovoltaic inverters can be overcome, resulting in lower costs, higher efficiency, and better reliability, and to a certain extent, solving the engineering application problems of photovoltaic inverters.

2.4. Structure optimization

Photoconductive Semiconductor Switch (PCSS) is a component with high-speed response and high repetition frequency in high-frequency and high-power applications. However, PCSS still has problems such as uneven electric field distribution, low voltage withstand capability, and slow response speed. The planar electrodes of PCSS can cause local breakdown due to electric field concentration, which greatly limits the power capacity and voltage withstand characteristics of PCSS. The thickness of the substrate, the direction of light excitation, and other factors also have certain impacts on the photoelectric output and response speed of PCSS.

To address these issues, the reverse-triggered electrode PCSS has emerged, which can improve the overall performance of PCSS [10]. The electrode configuration of the reverse-triggered structure can make the electric field distribution more uniform and effectively improve the phenomenon of electric field concentration, thereby enhancing the voltage withstand capability of PCSS. After adding the reverse-triggered structure, the maximum voltage withstand of PCSS has increased from 5.5kV to 8kV, significantly improving the high-voltage tolerance of PCSS devices. Due to the reduction in the volume of PCSS and the substrate thickness from 500μm to 50μm (Figure 5: (a) top view; (b) cross-section with a thickness of 500μm; (c) cross-section with a thickness of 50μm), the light-receiving area per unit area has increased, allowing more light energy to be converted into current, that is, increasing the photoelectric current density. Experiments have proved that the photoelectric current density has increased from 37 A to 41 A. Reducing the substrate thickness is an important way to improve the performance of PCSS. After thinning the substrate, under the same incident light irradiation, the response time of the laser during the triggering process will be shortened, the distribution of the photoelectric current will tend to be uniform, the photoelectric current density will increase, and the energy loss during the light excitation process will be reduced [10]. This is conducive to the advantages of PCSS devices, such as stable high-frequency operation, greater power output, and good working performance. Another advantage of the reverse-triggered structure is that it effectively solves the problem of excessive electric field strength at the electrode edges. The traditional planar electrode structure is prone to the phenomenon of high electric field strength at the electrode edges. When the applied voltage reaches a certain level, local breakdown between the electrodes may occur. After adopting the reverse-triggered structure, the electric field strength at the electrode edges can be effectively reduced, improving the stable working time of the device under high voltage and extending the service life and reliability of the device.

In summary, the reverse-triggered electrode structure solves the problems of uneven electric field and insufficient voltage withstand capability of PCSS devices during high-power use, and optimizes the electrode design, reduces the substrate thickness, and improves the distribution of the photoelectric current. The photoelectric output efficiency and response speed of PCSS devices have been greatly improved, and their voltage withstand capability has also been significantly enhanced. PCSS devices are likely to be used in high-power applications, such as microwave systems, radar systems, and other fields.

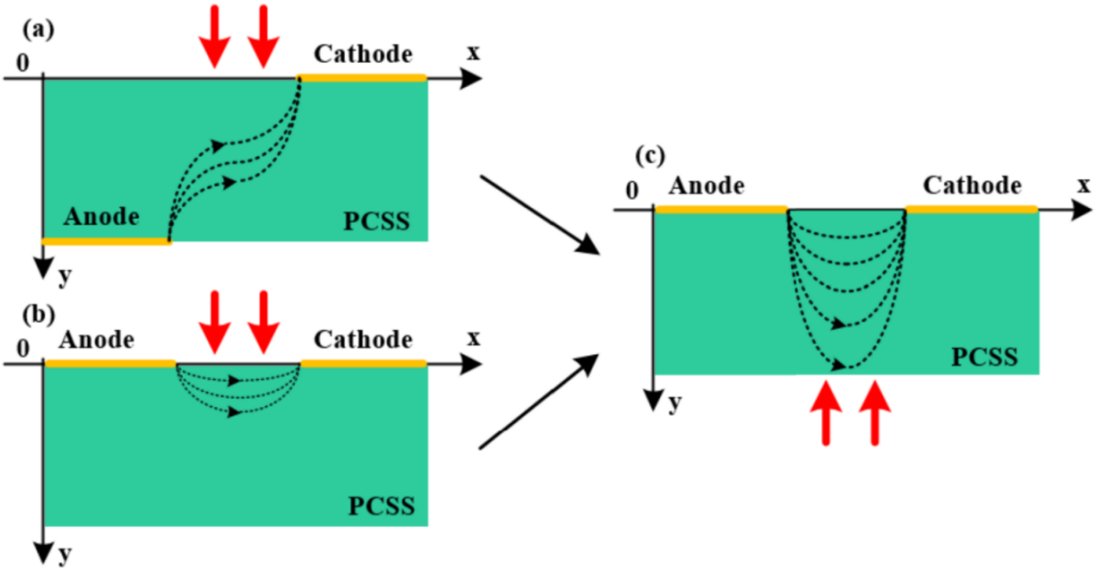
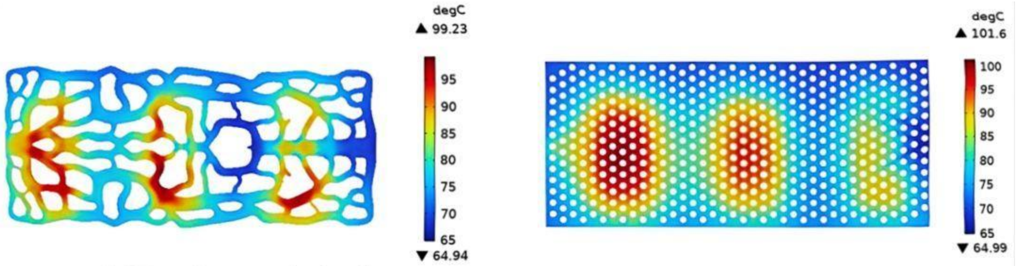


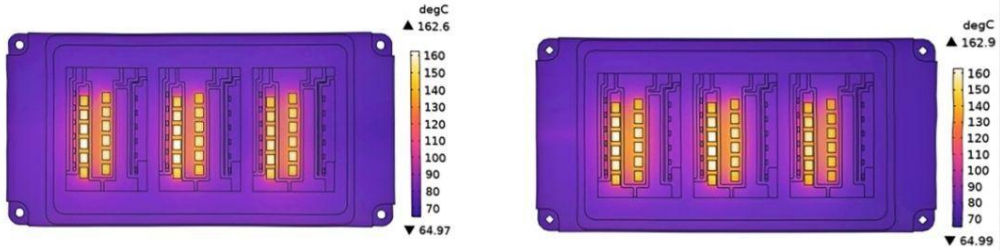
Figure 5. Schematic diagram of the inverted-triggered planar structure PCSS [10]

To enhance the heat dissipation performance of the power module in electric vehicles, especially for the power module based on SiC MOSFETs, a liquid-cooled heat sink design method based on topology optimization was studied [11]. Due to the advantages of SiC MOSFETs, such as higher operating temperature, higher switching frequency, and higher efficiency compared to traditional silicon-based insulated gate bipolar transistors (IGBTs), SiC MOSFETs are widely used in the switching of electric vehicle power inverters. However, the high-frequency operation of SiC MOSFETs leads to increased power loss and excessive temperature rise, posing significant risks to the inverter. The optimization design of the power module's heat dissipation system, particularly the heat sink, is of great importance. Liquid-cooled heat sinks are widely applied to the power modules of electric vehicles. Compared with traditional forced air cooling, liquid cooling can significantly reduce thermal resistance, volume, and increase heat flux. However, liquid-cooled heat sinks have problems such as high fluid flow resistance and poor heat dissipation performance. To address these issues, in this study, a pin-fin heat sink was utilized to construct a three-dimensional finite element model of the liquid-cooled heat sink, and a multi-objective topology optimization method was adopted to optimize the heat exchange performance and fluid dissipation energy of the liquid-cooled heat sink. The topology optimization simultaneously considered heat flow and fluid dissipation energy, and a weighting factor was introduced to balance the weights between the two. Through numerical simulation, it was found that under the working condition of a coolant volume flow rate of 85 kg/s, the heat sink optimized by topology optimization had better heat dissipation performance than the conventional heat sink. Compared with the pin-fin heat sink, the optimized heat sink had a 63.94% reduction in pressure drop and a 0.24% decrease in the junction temperature of the power module when the coolant flow rate was 14 L/min (Figure 6). This topology-optimized liquid-cooled heat sink can fully utilize the existing heat sink, improve heat dissipation performance, and reduce fluid flow resistance loss, thereby enhancing cooling efficiency. The optimized heat sink has good heat dissipation performance, and its maximum temperature is much lower than that of the conventional heat sink regardless of the coolant flow rate. Its flow resistance is much smaller than that of the conventional heat sink, and it has strong heat dissipation performance at high flow rates. Through technical analysis of the topology-optimized heat sink, it is known that it improves the overall heat exchange efficiency of the heat sink by using larger fins and inclined fins [11]. The topology-optimized heat sink can enhance the performance of the entire SiC MOSFET power module heat dissipation system, reduce energy loss, and improve heat dissipation performance, making it highly valuable for high-power electric vehicles. This research, by optimizing the design of the heat sink, not only improves the thermal management capability of the power module but also provides new ideas and methods for the design of future electric vehicle power module heat dissipation systems.



(a)Topology-optimized channel

(b)Pin fin channel



(c) SiC MOSFETs power module with topology optimization heatsink

(d) SiC MOSFETs power module with pin fin channel

Figure 6. Comparison of temperature distribution and junction temperature of power module between topology-optimized heat sink and pin fin heat sink under 14L/min working condition [11].

3. Discussion

For PVT method, increasing grain size and reducing grain boundary defects enhance the etching resistance and mechanical properties of SiC, making it suitable for high-power and long-life devices. However, it needs high requirements for equipment and is currently expensive, limiting its range of application. The in-situ strain control method can control the residual strain of the epitaxial film by adjusting the C/Si ratio to reduce defect density and improve film quality, which is more suitable for the precision and stability requirements of MEMS device films. The introduction of the MOS structure plays a very prominent role at the device level, as it can reduce leakage current and increase energy resolution by optimizing the thickness of the oxide layer. This also enables the application of SiC materials to more extreme environments such as neutron detectors. In addition to improving the material itself, in recent years, more research has been conducted on device structure design and heat dissipation to enhance the performance of SiC devices. A representative example is the PCSS structure with an inverted trigger electrode, which improves the electric field distribution and withstand voltage capability by optimizing the internal structure of the device, and achieves higher photocurrent density and faster response speed by thinning the substrate. It can be seen that the performance of the device can be significantly improved by the design of the device structure alone, without the need for additional material improvements or changes in the process.

From the perspective of the system level of semiconductor device construction, thermal management has become an important factor affecting the reliability of SiC devices. From the simulation study of the life reliability of Si/SiC hybrid inverters, it is found that SiC MOSFETs are prone to high-temperature damage due to high operating frequency and large switching losses, which has become the main bottleneck. However, methods such as life modeling simulation and optimizing the heat dissipation layout can greatly improve the device life without increasing costs. In addition, liquid-cooled heat sinks designed using topology optimization technology have higher heat exchange efficiency and lower pressure drop losses, and can be used in high-power applications such as electric vehicles. Therefore, the performance of SiC devices should not only be considered in terms of materials and interfaces, but also in terms of structural optimization and system coordination to achieve comprehensive performance improvement.

There are still some shortcomings in the improvement of SiC material growth, interface control, and system optimization. The lattice mismatch between Si and SiC substrates is as high as 19%. Although many excellent research results have been achieved in exploring new epitaxial preparation technologies to solve this problem, there are still many practical production process issues. Defects cannot be effectively suppressed, and device performance does not meet standards. The process parameters for industrialization are difficult, and the cost of PVT equipment is high. The strain control process has many steps and is highly uncontrollable. The reliability of the MOS structure cannot be verified under long-term extreme conditions. In actual use, SiC devices have problems such as packaging, electromagnetic compatibility, and short-circuit protection, which prevent them from being well applied in fields such as automobiles and photovoltaic power generation inverters. Future work can be carried out in the following aspects. First, it can develop new low-defect and high-uniformity SiC film growth technologies to solve the lattice mismatch problem. Second, it can find mutually coordinated solutions for material control and device structure optimization, and propose a multi-scale integration approach. Third, it can strengthen research on heat dissipation, packaging, and system reliability technologies, and improve the long-term stability of SiC devices in extreme environments from a system-wide perspective.

4. Conclusion

This study focuses on enhancing the performance of SiC materials and devices through breakthroughs in four key areas: material growth, interface engineering, device structure design, and system thermal management. By utilizing the PVT method and in-situ strain modulation, we have reduced defects in SiC films, leading to enhanced mechanical and electrical properties that are crucial for high-power applications. The introduction of MOS structures has optimized the interface, reducing leakage currents and enhancing device stability, while reverse-triggered electrodes and substrate thinning have improved the electric field distribution and voltage withstand capability of photoconductive semiconductor switches (PCSS). Additionally, our approach to thermal management, including topology-optimized liquid-cooled heat sinks, has significantly improved heat dissipation efficiency, extending the lifespan of SiC MOSFETs in high-frequency, high-temperature environments. The results demonstrate substantial improvements in SiC device performance, especially for electric vehicle power systems and renewable energy applications.

In summary, enhancing SiC performance requires a multi-scale, multi-level approach spanning materials, interfaces, device structures, and system thermal management. Integrated implementation of these strategies enables SiC-based devices to excel in high-temperature, high-frequency, and high-power environments, with promising applications in electric vehicles, photovoltaic inverters, and advanced electronic systems.

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