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A Comparative Study of Static CMOS and Transmission Gate Logic with Associated Optimization Techniques

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Abstract. The continuous advancement of complementary metal–oxide–semiconductor (CMOS) technology and the development of the Internet have made the optimization of logic gate design in digital integrated circuits face important challenges. This article systematically reviews some mainstream MOS logic structures - static CMOS, through-channel transistor logic (PTL), and transmission gate logic (TGL), and analyzes the latest progress in circuit optimization, manufacturing processes, and material/structure innovations. The article also compares and analyzes representative technologies including memory-in-circuit computing (CIM) based on MTJ/CMOS hybrid gates, wide bandgap semiconductors (4H-SiC, GaN, diamond), memristor logic, and FDM printed fluid logic gates. The study shows that static CMOS remains the preferred option for general design, while PTL/TGL have advantages in area and delay for specific functions due to threshold voltage loss or increased control complexity. Advanced optimization techniques, such as automatic write stop circuits, 673K post-annealing treatment, and unified NiOx dielectric integration, significantly improve power-delay performance and thermal stability. New material platforms further extend the application of logic gates to high-temperature and extreme electromagnetic environments. This comparison provides designers with reference suggestions for choosing the suitable logic structure under different application conditions.

Keywords: CMOS Logic; PTL; TGL; Logic Gate Optimization.

1. Introduction

As Internet of Things and artificial intelligence applications develop faster and faster, digital integrated circuits are facing increasingly severe challenges in terms of power consumption, delay, and reliability. As the basic building blocks, logic gates have developed quickly, making it difficult for designers to systematically select the appropriate circuits [1]. CMOS technology has extremely low static power consumption, complete voltage swing, and high noise tolerance, but N-input gates require 2N transistors, this needs more area. To deal with this issue, researchers have developed PTL and TGL, which use fewer transistors while maintaining complete swing [2].

The optimization work covers multiple levels. At the architecture level, computational internal storage (CIM) integrates metal-oxide-semiconductor (MTJ) with CMOS to solve the "memory wall" problem and achieve zero power consumption when it doesn't work [3]. At the manufacturing level, annealing can reduce the lag effect of 4H-SiC CMOS, and heterogeneous integration realizes the unified gate dielectric process of GaN nMOS and diamond pMOS [4, 5]. At the material level, memristors have a high switching ratio, two-dimensional materials support binary/trinary reconfiguration, and FDM-printed fluid gate provides a faster special logic gate design for special environments [6-8]. Also, at the logic level, the optimization method based on the decoder can identify reusable shared output groups, reducing the number of gate circuits by an average of 25% [9]. This paper provides a review and systematic comparison of static CMOS, PTL, and TGL, summarizing the new progress in circuit optimization, manufacturing technology, and material and structure innovations. By comparing aspects such as manufacturing cost, stability, delay, and power consumption, it provides general reference guidance for designers to select the appropriate logic gate type when they are facing different conditions.

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2. Optimization of Logic Gate Circuits

The performance optimization of logic gate circuits is one of the core tasks in digital integrated circuit design. Its goal is to achieve the optimal trade-off among power consumption, delay, and area under given conditions. Based on the research results from some excellent researchers, this paper systematically shows the optimization techniques for logic gate circuits focusing on delay and power consumption from optimization methods and typical cases.

2.1. Optimization of transistor size

The optimization of transistor size is the most basic and effective optimization method. For static CMOS inverters, by adjusting the channel width ratio of PMOS and NMOS, the rise delay and fall delay can be balanced. Chanda et al. demonstrated in a 45nm CMOS process that when the width of PMOS is twice that of NMOS, the inverter can achieve the minimum average propagation delay [10]. However, in the sub-threshold operating region, due to significant variations in carrier mobility and threshold voltage with temperature, size optimization also needs to consider the impact of temperature increase on the decrease in mobility on the delay characteristics. Barla et al. adopted a differentiated size strategy in the same process node [3]. They set the width of the write core transistor to three times the default value to support the superimposed flow of SHE and STT currents, while the remaining transistors maintained the default size. This strategy effectively optimized the current driving capability of the write path in the hybrid MTJ/CMOS circuit. Also, it was found that increasing the width of the pull-down transistor in the readout circuit can provide a faster discharge path and reduce the readout delay, but it will also lead to an increase in power consumption. A trade-off must be made between delay and power consumption. And Chinazzo et al. achieved 7% delay and 10% power reduction for PTL gates via cell selection optimization [1].

2.2. Optimization of Reading and Writing Circuits

In the design of digital circuits for implementing multi-output Boolean functions using decoders, consciously grouping the shared decoder outputs can make the outputs of the same logic gate to be reused by multiple functions, this can significantly reduce the total number of gates. Onai and Skopyk formalized this problem as follows: each function is composed of several terms, and the logic gates have fixed input ports. Through a density function, iterative selection of "bundled groups"(sets of terms appearing in two or more functions) is carried out, this function weighs the size, the number of benefiting functions, and the number of consumed gates, then selects the density-maximizing bundled group, removes its terms from all functions, and repeats this process until no shared outputs remain. For NOR and NAND inverters, the required number of gates is approximately twice that of non-inverters minus one. Tests on a large number of random four-function configurations show that this greedy algorithm can reduce the number of gates to 75% of the initial requirement within a millisecond-level running time, while brute-force search may need several years [9].

2.3. Geometric parameter optimization for fluid logic gates

Kendre et al. showed an optimization method for logic gates that goes beyond the traditional MOS device category. Based on FDM 3D printing technology, they used a flexible beam structure to achieve a fluid logic switch [8]. The design space of this device allows people to explore geometric parameters such as beam thickness, beam angle, beam length, beam spacing and beam spacing from the frame. Through parametric design, they successfully achieved two working modes, one is a single-stable mode for logic gates and another on is a double-stable mode for non-volatile storage. In the single-stable parameter configuration, the device can operate as a NOT gate, AND gate, OR gate and other logic gates and in the double-stable configuration, it can work as a non-volatile set-reset latch.

3. Optimization of manufacturing technology

Technology is developing every day. Optimizing manufacturing techniques is an important step in enhancing the performance, reliability, and integration level of logic gate circuits. As the process nodes of integrated circuits continue to shrink to the smaller scale, and with the emergence of wide bandgap semiconductors and emerging storage technologies, improvements in manufacturing processes have an increasingly profound impact on the power consumption, delay, and yield of logic gate circuits. We can't just keep using the traditional electrical components. New technologies have provided more easier ways when we design.

3.1. Post-Anneal Processing

Post-heat treatment is a useful method for improving device electrical performance. Rinaldi et al. systematically investigated the effect of 673K annealing on 4H-SiC CMOS inverters [4]. After annealing in ambient atmosphere for 30 minutes, the threshold logic voltage VM shifted 6.67% toward higher input voltage, and the hysteresis voltage ΔVH decreased from 0.2V to 0.15V. These changes are directly linked to individual MOSFET behavior: NMOSFET threshold voltage (VTH, N) increased by 6.93%, while PMOSFET threshold voltage (VTH, P) decreased by 11.15%, collectively working on the positive VM shift. At the same time, the hysteresis of NMOSFET and PMOSFET transfer characteristics reduced by 33.3% and 20.4%, this is why the inverter hysteresis reduction. The physical mechanisms include release of fixed oxide charge, altering flat-band voltages and threshold voltages, reduction of slow interface trap density, lowering hysteresis and decrease in SiO_2/4H-SiC interface defect density, improving PMOSFET subthreshold swing by 23.8% and peak channel mobility by 4.1%. Totally, the most significant improvement occurred after the first anneal, and the performance became stable after the second anneal, this confirms that annealing enhances device stability and repeatability.

3.2. High-K dielectric engineering and interface optimization

Perla et al. significantly improved the performance of the memristor device by adopting the carbon nitride (CN) functionalization modification strategy. After introducing CN into the silver-tin oxide (Ag_2SnO_3) nanoparticle system, the device changed from a single-write multiple-read (WORM) type storage behavior to a bistable memristor with stable low-conductance (LCS) and high-conductance (HCS) states, and its ON/OFF ratio reaches 1.2×10^4. The mechanism of CN's action is reflected in two aspects. CN acts as a barrier during the formation of silver filaments and increases the formation voltage from 4.6V to 6.8V. At the same time, the CN layer is encapsulated within the silver filaments, promoting the concentration of electric fields at the interface between the conductive filaments and the material, enhancing the Joule heating effect, and thereby makes the effective breakage of the filaments during the RESET process. The similar interface engineering also appears in the 4H-SiC CMOS process. After the 55nm gate oxide layer is thermally grown at 1300°C, it undergoes 1300°C gate oxide post-annealing (POA) in a NO environment can reduce the interface state density of SiO_2/4H-SiC [6].

3.3. Heterogeneous integration and unified dielectric strategy

Patil et al. successfully fabricated a CMOS inverter by integrating GaN nMOS and diamond pMOS through heterojunction integration technology [5]. The innovation of this technique lies in the use of a unified NiO_x gate dielectric and Ni gate metal, enabling the co-manufacturing of enhancement transistors on two different semiconductor platforms, significantly simplifying the process flow. Key technologies include: through ICP-RIE digital trench etching, part of the AlGaN/GaN heterojunction's AlGaN barrier layer is removed, combined with p-type NiO_x gate dielectric to bring the Fermi level closer to the valence band to deplete the two-dimensional electron gas (2DEG), thereby achieving enhancement operation. For the diamond pMOS, it is grown by MPCVD technology, and hydrogen plasma treatment and hydrogen atmosphere cooling are used to achieve hydrogen termination (H-termination), and through the surface transfer mechanism to form two-

dimensional hole gas (2DHG), while the combination of Ni/NiO_x shifts the Fermi level above the valence band, also achieving enhancement operation. In addition, to reduce the thermal budget to protect the H-terminal interface, pMOS uses a 6-nm thin layer of NiO_x, while nMOS uses 20-nm NiO_x, and through differentiated dielectric thickness, respectively achieve their target threshold voltages.

4. Comparative Analysis

Based on the analysis, this section conducts a systematic comparison of the above logic gate circuit technology routes from four key dimensions: cost, stability, latency, and power consumption. The comparing data from different CMOS technology is shown in Table 1.

Table 1. The comparing data from different CMOS technology

	Wide-Bandgap CMOS	CMOS Hybrid	FDM Fluidic Logic Gates	Conventional Si CMOS
Cost	High	Middle	Lowest	Low
Stability	Excellent(773K)	Middle	DNE	Bad
Delay	Middle ((~μs))	DNE	High (~ms-s)	Low (~ns-ps)
Power consumption	Middle	Low	Zero	Low

As the it shows, each technical solution has obvious trade-offs. Wide bandgap CMOS has excellent thermal stability and moderate power consumption, this makes it to be suitable for high-temperature and high-power scenarios that traditional silicon-based CMOS cannot work. For the memristor/CMOS hybrid logic, its non-volatility can achieve extremely low static power consumption and makes it to be highly recommended in memory computing applications with high energy consumption requirements. Although FDM fluid logic gates are slower in speed and larger in size, their unique advantages lie in zero power consumption and complete immunity to electromagnetic interference, making them suitable for special environments such as strong radiation, magnetic fields and explosive hazards. Because of the low cost, high speed, and mature ecosystem, traditional silicon-based CMOS is still the first choice to be considered for general applications.

5. Conclusion

In conclusion, the applicable scenarios for each technology route are clearly recommend. Wide bandgap CMOS is suitable for high-temperature and high-reliability applications. The memristor/CMOS hybrid is suitable for low-power on-chip computing. The FDM fluid logic gates provide a non-electronic alternative solution for extreme electromagnetic environments. At the logical level, by identifying reusable shared output groups, the method of implementing multiple Boolean functions using decoders was optimized, resulting in a 25% reduction in the number of logic gates. The integration of multiple technologies in the future will become an important direction for the innovation of logic gate circuits. The design of logic gate circuits is moving towards diversification, heterogeneity and intelligence. Different logical styles have their own applicable scenarios, manufacturing processes and material innovations are constantly expanding the performance boundaries, and the integration of emerging storage and computing technologies has opened new possibilities for the development of logic gate circuits. Also, the diversification can provide more and more different situations for different logic gates. There may be more and more situations that need the different ways of special logics gate to work together to build the circuit. The passage can provide some help to find similarities between different ways and make it easier to be with others.

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