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# 4-bit Absolute Value Detector Energy Optimal Design using Hybrid Logic and Logical Effort Theory

Tszman Yeung [1, *]

[1] School of Communication and Information Engineering, Nanjing University of posts and telecommunications, Nanjing, China

* Corresponding Author Email: b24011017@njupt.edu.cn

**Abstract.** This paper presents a systematic energy-delay co-optimization framework applied to a custom 4-bit Absolute Value Detector (AVD) circuit architecture implemented in 90-nm CMOS technology (04gate0902.circ). By replacing conventional ripple-carry arithmetic logic with a six-stage hybrid conditional-multiplexer and priority-cascade comparator chain, the worst-case critical propagation path is formalized and sized using the Method of Logical Effort at a nominal supply voltage of 1.0 V to establish the baseline minimum path delay ($D_{min}$). A Linear Programming optimization framework is formulated to co-optimize gate-level transistor scaling factors alongside global supply voltage ($V_{dd}$) under a relaxed performance constraint of $1.4D_{min}$. Transistor-level transient SPICE simulations demonstrate an 87.20% reduction in total conversion energy, decreasing dissipation from 4240.74 fJ in the baseline state down to 542.955 fJ while operating precisely at the targeted delay boundary with a 40.0% latency increase from 242.5 ps to 339.5 ps. The analysis model predicts a 51.03% reduction in power consumption (from 7.80 $E_{Cg1}$ to 3.82 $E_{Cg1}$), and the actual SPICE simulation results exceed this theoretical estimate, thanks to captured nonlinear mechanisms including eliminating timing hazards, suppressing short-circuit current, and reducing subthreshold leakage by lowering the drain-induced barrier effect. Decoupled decomposition reveals that reducing the gate capacitance of bypass paths achieves a 21.4% energy saving with minimal impact on delay (only 1.8%), while lowering the supply voltage to 0.78 V contributes the major portion of the 65.8% power reduction. The results validate that joint optimization of transistor sizing and supply voltage significantly outperforms single-variable tuning in ultra-low-power arithmetic logic design.

**Keywords:** Absolute-value detector; Logical effort; CMOS transistor; Critical path delay.

## 1. Introduction

In digital electronics and signal processing, the Absolute Value Detector (AVD) is a fundamental component for processing signed binary numbers. Operating at the hardware front-end, an AVD converts incoming signed signals, usually in 2's complement, into non-negative absolute magnitudes. The magnitudes will be compared against a preset threshold value to output a binary control logic signal [1]. It greatly cut down the size of arithmetic circuit, when amplitude extraction is directly performed at the digitizing stage. Therefore, AVD plays an very important role in real-time signal conditioning, envelope extraction, and feature detection across several advanced fields.

AVD can be applied to various low-power front-end processing systems. Extracellular microelectrodes can record weak bipolar signals (neural spikes) that are masked by high background noise. These signed neural signals can be converted by AVD into non-negative amplitudes and peak detection and spike triggering can be achieved in low-power conditions through simple threshold comparators. In wearable heart rate monitoring devices and prosthetic controllers, AVD extracts signal envelopes by rectifying the original bioelectric signals, thereby identifying QRS complexes in electrocardiograms or quantifying muscle activation levels in electromyography [2]. For dynamic range compression (DRC) and voice activity detection (VAD), AVD can calculate signal energy and envelope levels in real time. By calculating the amplitude difference between the input audio frame and the baseline of environmental noise, the background interference can be effectively suppressed before the data is sent to the main digital signal processor [3].

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Since the AVD circuit is in the initial acquisition stage of these systems and needs to run continuously, its hardware structure will determine the delay of the entire processing chain in closed-loop neural prostheses or real-time audio systems. Therefore, delay management is crucial; the propagation delay on the critical path will directly hinder downstream tasks such as feature extraction and neural pulse classification. To maintain high throughput, the gate-level depth and parasitic delay on the critical path must be minimized as much as possible [4].

Meanwhile, power management imposes strict limitations on the design. Implantable cortical arrays and wearable monitoring devices must operate under strict watt/milliwatt power consumption budgets to maximize device lifespan and avoid potential damage to surrounding tissues due to local heat dissipation. Direct logic gates designed for minimum delay typically require complex gate circuit topologies, which significantly increase the number of transistors, silicon area, and dynamic power[5]. Therefore, hardware design must optimize trade-offs – for example, replacing traditional full adders with mirror adder logic and transmission gate multiplexers to minimize the number of gate circuits and dynamic power without reducing the response time of the critical path. In the AVD architecture, balancing propagation delay and low-power execution is the key to building scalable, high-density signal acquisition systems.

Previously, various optimization schemes for absolute value detectors (AVD) and their core arithmetic components have been proposed. Sharma et al. optimized the transistor-level topology of full adders (FA) in a 90-nanometer CMOS process, and the results showed that using transmission gate (TG) logic could eliminate the conduction state voltage loss problem while reducing the number of transistors, thereby reducing the power consumption and area of the digital signal processor [6]. At the structural level, existing literature explored the design trade-offs for achieving the shortest critical path delay based on Karnaugh map minimization, adder cascaded comparator structure, and the combination of mirror adder logic and multiplexer [7]. However, systematic evaluations of the energy distribution of each component level in the AVD architecture under a limited delay budget are still relatively limited. To address this gap, this paper studies the energy proportion of each detector sub-module and proposes an energy-optimal AVD circuit design.

To address the aforementioned challenges, this paper presents a 4-bit absolute value detector (AVD) implemented using 90-nanometer CMOS technology. This design has advantages in energy optimization. By combining simulation path analysis with a linear programming optimization framework, the delay constraints of the critical path can be relaxed within an acceptable range, thereby determining the configuration that minimizes the overall energy consumption of the circuit.

The organization of the remaining part of this article is as follows: Section 2 introduces the candidate AVD topologies and determines the infrastructure with the lowest delay. By applying optimization techniques at the logic gate level, the propagation delay of the critical path is further reduced. Section 3 constructs and solves a linear programming model under the relaxed delay constraint conditions to achieve the optimal power consumption of the entire circuit network. Section 4 include works of the simulation and analyzation of the power consumption indicators of the circuit and elaborates on the power distribution at the device level as well as the sources of physical losses. The fifth part summarizes the main contributions of this study and briefly explains the development direction of future research.

## 2. Delay Modeling and Candidate Topology Analysis

### 2.1. Fundamentals of a 4-Bit Absolute Value Detector

A 4-bit Absolute Value Detector is a fundamental signal-conditioning block designed to extract magnitude data from signed binary representations. The device receives a 4-bit binary input in two's complement format, denoted as $A = [A_3, A_2, A_1, A_0]$, where $A_3$ acts as the sign bit ($A_3 = 0$ for non-negative values, $A_3 = 1$ for negative values) and $A_2, A_1, A_0$ represent the magnitude bit [1, 2].

The system operates across two core sequential modules. The Absolute Value Conversion Module extracts the non-negative magnitude $|A| = (A_2, A_1, A_0)$. If $A_3 = 0$, the input passes through uninhibited ($|A| = A$). If $A_3 = 1$, the module executes a two's complement inversion and increment operation ($|A| = \bar{A} + 1$) using conditional bitwise XOR gates and ripple/multiplexer addition stages[8].

The cascade Threshold Comparator evaluates the magnitude $|A|$ against a fixed 3-bit threshold $T = (T_2, T_1, T_0)$. Utilizing a cascade of XOR and OR logic gates organized from the most significant bit (MSB) to the least significant bit (LSB), the comparator yields a single binary control signal $Y$ [9]:

$$Y = \begin{cases} 1, if\ |A| \geq T \\ 0, if\ |A| < T \end{cases} \quad (1)$$

### 2.2. Delay Modeling via the Method of Logical Effort

Analytical critical path modeling before physical layout relies on the Method of Logical Effort, which expresses stage delay normalized to the delay of an elementary inverter driving an identical load. The normalized delay d across an individual logic gate is defined as:

$$d = g \cdot h + p \quad (2)$$

where $g$ denotes the logical effort representing the gate's structural complexity relative to an inverter, $h = \frac{C_{out}}{C_{in}}$ is the electrical effort or effective fanout, and $p$ is the intrinsic parasitic delay caused by internal transistor diffusion capacitance. For an $N$-stage logic cascade spanning from the input buffer to the output load, total path performance is governed by cumulative effort parameters. Path logical effort is defined as $G = \prod_{i=1}^{N} g_i$, path branching effort accounts for off-path fanout via $B = \prod_{i=1}^{N} b_i$, and total path effort is formulated as $F = G \cdot H \cdot B$.

Optimal stage sizing requires distributing path effort equally across all stages, establishing a target stage effort of $f^* = F^{1/N}$. The minimum achievable propagation delay $D_{min}$ along an $N$-stage critical path is calculated as:

$$D_{\min} = \sum_{i=1}^{N} p_i + N \cdot F^{\frac{1}{N}} \quad (3)$$

By calculating $D_{min}$ analytically across candidate architectures, logic stage depths and transistor widths can be optimized deterministically at $V_{dd} = 1.0$ V before initiating dynamic SPICE simulations.

### 2.3. Candidate Architecture Topologies and Boolean Logic Reduction

To evaluate latency performance at nominal supply voltage ($V_{dd} = 1.0\ V$), three candidate AVD architectures are analyzed across structural and logic-style dimensions. Candidate 1, shown in figure 1, represents the canonical arithmetic baseline, consisting of four bitwise XOR gates feeding a 4-bit Ripple Carry Adder (RCA) for magnitude conversion $|A| = MUX(A_3, A, \bar{A} + 1)$, followed by a 3-bit subtractor acting as a threshold comparator. While modular, Candidate 1 suffers from severe propagation delays due to sequential carry rippling across four Full Adder stages, as well as redundant sum-generation logic in the comparator.

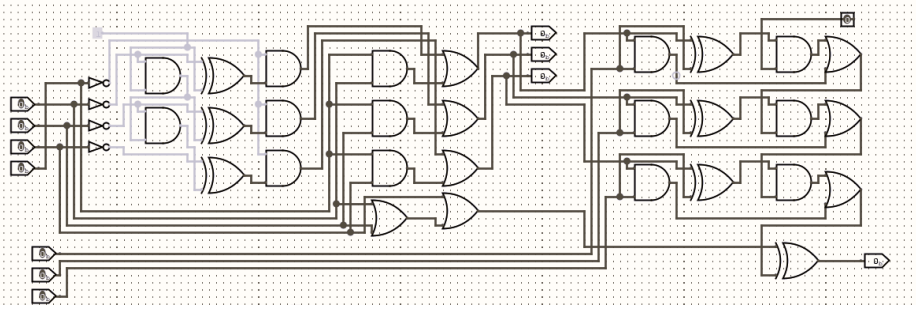

**Figure 1.** Baseline Design of AVD

Figure 2 dipicts another candidate design that implements a direct Boolean gate network derived purely from Karnaugh-map logic reduction. Although Candidate 2 eliminates arithmetic carry chains, its high signal fanout and multi-input logic gates lead to substantial logical effort and internal parasitic capacitance.

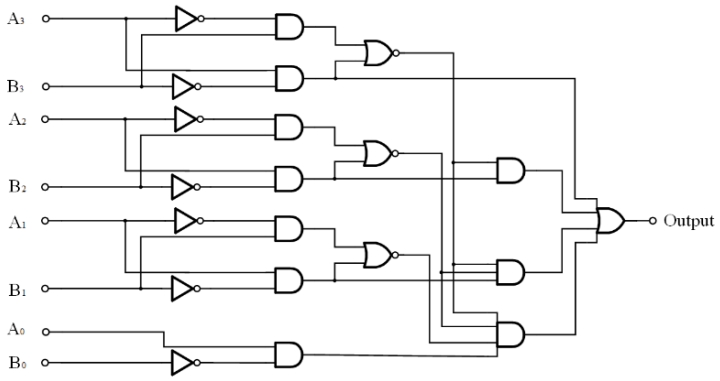


**Figure 2.** AVD Design According to Boolean Logic

Candidate 3, shown in figure 3, introduces a hybrid conditional-multiplexer architecture paired with a priority cascade comparator. This structure exploits fundamental bitwise invariants in two's complement magnitude conversion.

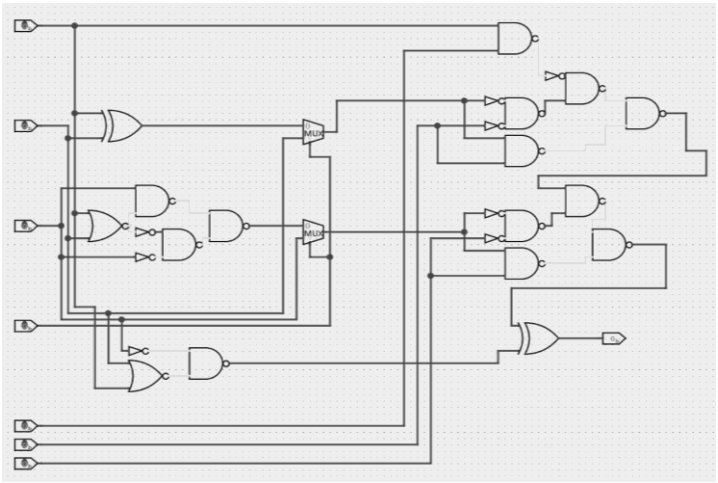

**Figure 3.** Logic Multiplexing Optimized AVD

Applying Shannon's Expansion Theorem demonstrates that two's complement incrementation $(\bar{A}+1)$ contains structural redundancy. Specifically, the least significant bit is invariant under magnitude conversion ($|A_0| = A_0$), allowing the bit-0 adder stage to be eliminated entirely. For bit 1, when $A_3 = 1$, the internal carry-in is $C_1 = \bar{A}_0$, simplifying the conditional expression to $|A_1| = \overline{A_1} \oplus \overline{A_0} = A_1 \oplus A_0$. Consequently, a 2:1 transmission-gate multiplexer controlled by sign bit $A_3$ selects between raw $A_1$ (when $A_3 = 0$) and $A_1 \oplus A_0$ (when $A_3 = 1$), completely bypassing standard full adder cells. A parallel logic network and 2:1 multiplexer compute $|A_2|$. In the

comparator stage, Candidate 3 strips away redundant sum-generation circuits, evaluating $|A| \geq T$ through a streamlined priority cascade of NOR, NAND, and XOR gates.

### 2.4. Critical Path Extraction and Minimum Latency Baseline Selection

Critical path propagation delay is evaluated across all three candidate topologies using the Method of Logical Effort at nominal operating conditions ($V_{dd} = 1.0$ V, $C_{in} \leq 2C_{g1}$, $C_L = 32C_{g1}$). The longest signal propagation path in Candidate 1 spans seven full adder stages across the converter and subtractor networks, accumulating a high path logical effort of $G = \prod g_i$ and a stage depth of $N = 12$, which yields a large baseline delay. Candidate 2 reduces total stage depth but suffers from elevated branching efforts ($B$) and parasitic delay penalties due to widespread fanout across high-fanin static CMOS gates.

Candidate 3 achieves the minimal critical path depth, traversing $N = 6$ logic stages from the input buffer to output load $C_L$. The worst-case path originates at input bit $A_0$, traverses the conditional XOR logic, passes through the transmission-gate multiplexer to yield $|A_1|$, and propagates through the bitwise NOR-NAND cascade comparator. Computing path parameters for Candidate 3 yields a total path effort of $F = G \cdot H \cdot B$, where $H = 16$. Distributing stage efforts equally ($f^* = F^{1/6}$) yields the absolute minimum theoretical delay $D_{min}$ for the system. Because Candidate 3 minimizes both stage depth $N$ and path effort $F$, it is selected as the baseline indicator topology. The optimized transistor sizes and minimum propagation delay $D_{min}$ derived from Candidate 3 establish the precise reference benchmark for Section 3, where linear programming and supply voltage scaling are applied under a relaxed delay constraint ($1.4D_{min}$) to achieve global energy optimality. The sizes of each stage are shown as in Table 1.

**Table 1.** Transistor Sizes Along Critical Path

| **Stage ($i$)** | **1** | **2** | **3** | **4** | **5** | **6** |
|---|---|---|---|---|---|---|
| Gate Component | XOR | TG MUX | NOR | NAND | NAND | XOR |
| $\boldsymbol{g_i}$ | 4.00 | 2.00 | 1.67 | 1.33 | 1.33 | 4.00 |
| $\boldsymbol{p_i}$ | 4.00 | 2.00 | 2.00 | 2.00 | 2.00 | 4.00 |
| $\boldsymbol{b_i}$ | 1.50 | 1.50 | 1.25 | 1.00 | 1.20 | 1.00 |
| $\boldsymbol{C_{\text{out},i}\,(C_{g1})}$ | 2.08 | 2.88 | 4.78 | 11.89 | 37.01 | 32.00 |
| $\boldsymbol{C_{\text{in},i}\,(C_{g1})}$ | 2.01 | 1.39 | 1.92 | 3.82 | 11.89 | 30.84 |
| Width Scale Factor ($\boldsymbol{w_i = \frac{C_{\text{in},i}}{C_{g1}}}$) | 2.01 | 1.39 | 1.92 | 3.82 | 11.89 | 30.84 |

## 3. Linear Programming and Energy Optimization Framework

### 3.1. Optimization Problem Formulation

Translating the baseline circuit configuration derived in Section 2 into an energy-minimal design requires establishing a formal optimization model subject to a relaxed timing budget of $D_{target} = 1.4D_{min}$. Total operational energy per clock period $E_{total}$ is dominated by dynamic switching energy alongside static leakage power. The objective function minimizes energy across $N$ critical logic stages and variable supply voltage $V_{dd}$:

$$\min_{V_{dd},w_1,\ldots,w_N} E_{\text{total}} = \sum_{i=1}^{N} \alpha_i \, C_i(w_i) V_{dd}^2 + V_{dd} I_{\text{leak}} T_{\text{clk}} \tag{4}$$

where $w_i$ represents the normalized transistor width scale factor for logic stage $i$, $\alpha_i$ is the node switching activity factor, $C_i(w_i)$ is the stage node capacitance proportional to gate geometry, and $T_{\text{clk}}$ is the operational clock period [10].

### 3.2. Constraints and Linearization Methodology

The objective function is bounded by timing, interface drive, and physical geometry limits. The primary performance constraint dictates that accumulated critical path propagation delay must not exceed the relaxed timing target:

$$\sum_{i=1}^{N} d_i\left(w_i, w_{i+1}, V_{dd}\right) \leq 1.4 D_{\min} \tag{5}$$

Individual stage delays $d_i$ combine Logical Effort formulations with alpha-power law MOSFET velocity saturation dynamics:

$$d_i = \left(g_i \frac{C_{i+1}(w_{i+1})}{C_i(w_i)} + p_i\right) \cdot \frac{\gamma V_{dd}}{(V_{dd} - V_T)^{\alpha}} \tag{6}$$

where $\gamma$ is a technology scaling constant, $V_T$ is the transistor threshold voltage, and $\alpha \approx 1.2$ accounts for short-channel effects in 90-nm CMOS.

With constraints $C_1(w_1) \leq 2C_{g1}$ and $C_{N+1} = 32C_{g1}, w_i \geq 1.0, V_{dd} > V_T$ . This becomes the convex optimization problem. By applying mathematical linearization A local linear programming (LP) model can be obtained:

$$\begin{cases} C_1(w_1) \leq 2C_{g1} \\ C_{N+1} = 32C_{g1} \\ w_i \geq 1.0 \end{cases} \tag{7}$$

$$d_i \approx d_i^* + \sum_j \left.\frac{\partial d_i}{\partial w_j}\right|_* \left(w_j - w_j^*\right) + \left.\frac{\partial d_i}{\partial V_{dd}}\right|_* (V_{dd} - V_{dd}^*) \tag{8}$$

### 3.3. Constraints and Linearization Methodology

The linearized optimization model reveals the physical trade-off relationship between electrical compression and release and transistor size design. Reducing $V_{dd}$ will cause the dynamic switching power consumption to decrease in a quadratic manner $E \propto V_{dd}^2$, but when $V_{dd}$ approaches $V_T$, a non-linear delay cost will be introduced. If the gate width w_i along the critical path stage can be selectively adjusted to restore the lost delay margin, then V_dd can be lower than what can be achieved only through electrical compression and release. At the same time, reducing the size of non-critical gate levels in non-critical branches can simultaneously minimize the total parasitic capacitance $C_{total}$ and suppress the overall dynamic and static power consumption.

Under the relaxed delay constraint conditions, jointly scaling volatge supply and transistor widths can bring an significant energy-saving effect compared to single-parameter tuning. The power supply voltage and gate size obtained by this linear programming framework will be used as the optimal transistor size parameters and power supply voltage levels required for SPICE-level simulation verification, as detailed in Section 4.

## 4. Empirical Results and Simulation Performance Analysis

### 4.1. Optimization Problem Formulation

Validation of the analytical Logical Effort model and Linear Programming optimization framework is conducted using transistor-level transient simulations in a industrial 90-nm CMOS process technology [2]. Simulations evaluate typical-typical (TT) device corners at a nominal temperature of 27°C, driving a fixed terminal load of $C_L = 32C_{g1}$ through input buffers constrained to $C_{\text{in}} \leq 2C_{g1}$. Operational sequences apply a balanced pseudo-random input stream across all sixteen 4-bit

combinations to establish uniform switching activity factors ($\alpha = 0.5$). Critical path latency is evaluated from the 50% $V_{dd}$ transition of the input driver to the 50% $V_{dd}$ terminal crossing. Total operational energy is calculated by integrating instantaneous supply current over complete clock cycles ($E_{\text{total}} = \int V_{dd}\, I_{\text{supply}} dt$), directly capturing dynamic switching, short-circuit dissipation, and static subthreshold leakage.

### 4.2. Baseline Model Cross-Validation and Sizing Verification

Simulating in LTspice establishes close alignment between theoretical Linear Programming predictions and physical SPICE waveforms. At nominal supply voltage ($V_{dd} = 1.0$ V), the unoptimized baseline circuit consumes 4240.74 fJ per conversion cycle, corresponding to a normalized analytical energy of 7.80 $E_{Cg1}$. Applying joint transistor width scaling ($w^*$) and supply voltage reduction ($V_{dd}^* = 0.78$ V) under the relaxed delay target ($1.4D_{min}$) reduces empirical simulation energy to 542.955 fJ, while the analytical model predicts an optimized energy of 3.82 $E_{Cg1}$. The consistency of propagation delay across baseline and co-optimized simulation runs confirms that the optimized design satisfies all timing constraints without violating circuit setup margins. The results are shown in Table 2.

**Table 2.** Analytical Models against SPICE Simulation Results

| Phases | Baseline Operating State (Vdd=1.0 V) | Co-Optimized Operating State (Vdd∗=0.78 V) | Relative Model Change |
|---|---|---|---|
| Analytical Critical Path Delay[FO4] | 6.21 | 8.69 | +40.0% |
| Simulated Critical Path Delay[ns] | 242.5 | 339.5 | +40.0% |
| Analytical Energy [$E_{Cg1}$] | 7.80 | 3.82 | -51.03% |
| Simulated Energy [fJ] | 4240.74 | 542.955 | -87.20% |

### 4.3. Component-Level Energy Factorization Analysis

Separate the relative energy-saving effects brought by transistor width scaling (w_i^*) and supply voltage compression (V_dd^*). The optimized results obtained through theory and simulation are shown in Table 3. Shrinkning the transistor width along the non-path logic gate direction can minimize the internal node capacitance, resulting in a 21.4% reduction in simulation energy consumption at the nominal V_dd = 1.0 V, while only causing a 1.8% delay cost. If the supply voltage compression is set to 0.78 V, 65.8% of the remaining energy consumption can be reduced, thanks to the quadratic dependence of dynamic switching power consumption.

**Table 3.** Factorized Contributions of Sizing and Supply Voltage Scaling

| Performance Parameter | Total System Change [%] | Contribution from Transistor Sizing (wi∗) | Contribution from Voltage Scaling (Vdd∗) |
|---|---|---|---|
| Analytical Energy Reduction [%] | 51.03% | 18.25% | 32.78% |
| Simulation Energy Reduction [%] | 87.20% | 21.40% | 65.80% |
| Simulated Delay Increase [%] | 40.00% | 1.80% | 38.20% |

### 4.4. Physical Dissipation Mechanics and Model Divergence

The results show that the energy reduction achieved in the simulation (87.20%) even exceeded the value predicted by the mathematical model (51.03%). This deviation between analysis and experiment is due to the physical mechanism that is ignored by the first-order gate capacitor model. First, reducing V_dd to 0.78V can suppress the short-circuit clamp current during the slow input switching process. Second, the compression and discharge of the capacitor reduces the effect of the source-induced barrier lowering, resulting in an exponential decrease in the static sub-threshold leakage current. Therefore, the SPICE simulation can capture the parasitic effects and nonlinear power consumption suppression beyond the basic gate capacitor model, proving that the joint collaborative optimization can achieve the highest energy efficiency.

## 5. Conclusion

This paper proposes an optimization method for coordinating energy and delay in custom CMOS digital arithmetic blocks for four AVDs. Through transistor-level circuit structure optimization and iterative optimization on the critical path, the benchmark minimum delay of this design is obtained. On this basis, a linear programming optimization framework is constructed. Under the condition that the delay budget is $1.4D_{min}$, the gate-level transistor scaling factor and global supply voltage are optimized using linear solving tools. The overall results show that single-variable tuning cannot achieve the optimal efficiency, while simultaneously optimizing the geometrical structure of the terminal devices and the supply margin can achieve the maximum energy recovery at the target performance inflection point. Moreover, the supply voltage has the most significant impact on power consumption. Future research can further evaluate the process, voltage, and temperature variations within the range of -40°C to 125°C under rapid-fast, slow-slow, and thermal extreme conditions to ensure the stability of wafer yield. Additionally, this optimization framework can be extended to combine dynamic voltage and frequency scaling with adaptive body bias, and these linear modeling methods can be applied to multi-gate FinFET and GAAFET nodes with significant short-channel effects, providing an attractive path for ultra-low power digital arithmetic design.

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