Transactions on Computer Science and Intelligent Systems Research
ISSN: 2960-1800, eISSN: 2960-2238 | Volume 14
TPCEE 2026

Parameter Sensitivity of Delay–Energy Trade-Offs in a CMOS 4-Bit Absolute-Value Computation Circuit with Threshold Detection Using LTspice

Han Zhang [1, *]

[1] Xi'an Jiaotong-Liverpool University, Suzhou, Jiangsu 215123, China

* Corresponding Author Email: Han.Zhang23@student.xjtlu.edu.cn

Abstract. This paper investigates the delay–energy trade-off and parameter sensitivity of a complementary metal-oxide-semiconductor (CMOS) 4-bit absolute-value computation circuit with threshold detection using transistor-level LTspice simulation. An optimized mirror-adder-based architecture is adopted as the reference structure, and its performance is systematically evaluated under different transistor-sizing and supply-voltage conditions without modifying the circuit topology. Three experimental groups are established to characterize the baseline performance, determine the minimum-delay configuration, and identify an energy-efficient operating region under a timing constraint. The reference circuit achieves a worst-case propagation delay of 148.262 ps with an energy consumption of 13.663 pJ. Through critical-path transistor sizing in Group B, the minimum delay is reduced to 85.560 ps, although the energy consumption increases to 16.950 pJ, demonstrating that delay-oriented optimization alone cannot guarantee energy efficiency. Group C further explores energy reduction by jointly adjusting transistor dimensions and supply voltage while maintaining the delay constraint derived from the minimum-delay condition. The optimized operating point is obtained at V_{DD} =0.828V, achieving a worst-case delay of 119.761 ps and an energy consumption of 8.769 pJ, corresponding to a 48.3% reduction compared with the minimum-delay configuration. The results demonstrate that transistor sizing and supply-voltage scaling exhibit different parameter sensitivities and should be jointly considered for delay-constrained energy optimization. This study provides practical design insights into low-energy CMOS combinational circuits.

Keywords: CMOS absolute-value detector; transistor sizing; parameter sensitivity; supply-voltage scaling; delay–energy trade-off.

1. Introduction

Excellent digital integrated circuits designs are placing greater emphasis on propagation delay and energy consumption, especially for CMOS VLSI circuits [1]. The magnitude of an input signal should be controlled within a predefined threshold to better reach the standard of delay and energy, this is necessary for embedded systems, digital processing and neural signal detection. Under this background, the absolute-value detector can realize its combinational logic to deal with practical issues. An absolute-value circuit can generate the magnitude representation of the input, and compare threshold to detect an absolute value. A systematic optimization for the threshold detection function allows it to benefit spike detection in neural signal processing [2].

In conventional design, the detector circuit separates the detection process into absolute-value extraction and comparison with a predefined threshold. The circuit architecture gets complex with the repeat use of multiplexers, inverters, adders and comparators. A 4-bit two's complement input needs multiple logic units to realize these functions, as well as inevitable increase of propagation delay and energy consumption. But the structure can occur function overlaps as the the circuit might reach the same function with less components. Ge et.al. proposed an optimized design for the carry-generation stage of the 4-bit absolute-value detector [3]. This approach aims to use mirror adder instead of the conventional full-adder structure, to reduce the use of transistors, and gain shorter delay, less energy consumption at the same time. The resulting core architecture consists six inverters, three

Content from this work may be used under the terms of CC BY-NC 4.0 licence (https://creativecommons.org/licenses/by-nc/4.0/).
Published by Warwick Evans Publishing.

multiplexers and tree mirror-adder carry units. This paper developed the mirror-adder design and further applied logical effort optimization to determine suitable transistor sizing. The optimized circuit will then provide data for parametric sensitivity investigation.

The purpose of parametric sensitivity analysis is to find balanced specifications and parameters for practical implementation. In CMOS circuits, propagation delay and energy consumption are closely related indicators for performance, particularly when using swing restored technique in transistor-level arithmetic circuits [1]. One angle to optimize is to enhance driving capability by increasing transistor dimensions. This approach reduces propagation delay at the cost of energy consumption, because it results in increasing parasitic capacitance. Similarly, sacrificing delay by aggressive voltage reduction saves energy, leading to tighter timing constraints [4]. Therefore, this experiment will repeatedly alter parameter conditions to identify proper transistor sizing and supply voltage variations, and summarize component performance curves with simulation data.

Driven by this motivation, this study focuses on delay-energy trade-off and parameter sensitivity of a 4-bit CMOS absolute-value detector with transistor-level LTspice simulation. The optimized design in the second paragraph will undergo a systematic process. With the reference performance baseline constructed, it reveals critical-path analysis, transistor sizing adjustment, and minimum-delay operating point determination. Based on these information, this experiment will then adjust key design parameters including transistor dimensions and supply voltage to simulate propagation delay and energy consumption. Finally, by analyzing the delay-energy characteristics, the operating regions of energy and efficient can be explored. To demonstrate the optimization process, this paper developed a comparative analysis between different systematic parametric experiment groups. Generally, this work aims to characterize the delay-energy trade-off and parameter sensitivity of CMOS absolute-value detectors and provide design insights for similar low-power combinational logic circuits.

2. Theoretical Foundations and Scheme Analysis

2.1. Digital Logic Principles of a 4-bit Absolute-Value Detector and Device Characteristics

A CMOS absolute-value detector is a combinational logic circuit that extracts amplitude from signed binary inputs. It reflects sign detection results and translates input information into magnitude values. In digital systems, two's complement is a standard representation. For an n-bit two's-complement number, the most significant bit (MSB) indicates the sign, with logic '1' indicating a negative value while logic '0' stands for an non-negative value. To implement this logic, the circuit demands blocks in charge of path selection and data conversion.

Take 4-bit two's complement input $A = A_3A_2A_1A_0$ as an example. The sign bit of this input is A_3, A_2, A_1 and A_0 are the data bits. When MSB is 0, the absolute value remains the same as the original input, that is:

$$|A| = A \tag{1}$$

When MSB is 1, this two's complement must be performed bit inversion of the original data, followed by an increment by one. This process can be expressed as:

$$|A| = \bar{A} + 1 \tag{2}$$

Where $\bar{A}$ represents the bitwise complement of the original input. Absolute value is operated through the cooperation of several basic logic modules. Commonly, the sign bit module controls the selection of processing paths; multiplexers switch between raw input data and converted magnitude values according to the control state to be '1' or '0'. These mechanisms reveal that the detector circuit is built upon sign detection, data reconstruction and arithmetic processing stages. Logic conversion units and arithmetic modules should be equipped to achieve these functions, while further increases

hardware overhead. Previous CMSO logic studies have verified that circuit topology, internal-node activity and signal-path complexity can affect propagation delay and performance metrics related to energy [5].

Besides these considerations, the switching behavior of MOS transistors influences the circuit performance. In standard CMOS topology, PMOS and NMOS devices form the networks that charge and discharge to determine output transitions, this capability depends directly on and node charging or discharging behavior, and is affected by transistor dimension settings [6]. Changing this parameter is still a balance between delay and energy, if transistor width increases, circuit delay is reduced while the total driving is enhanced. However, excessive sizing might offset part of the performance benefit. This sizing trade-off motivates the use of selective rather than uniform transistor enlargement in delay-sensitive CMOS paths [7].

2.2. Conventional Absolute-Value Detector Architecture, and transistor-Level Implementation

As described in Section 2.1, the MSB controls the sign-dependent processing path: positive inputs bypass magnitude conversion, whereas negative inputs undergo two's-complement magnitude conversion. Conventional absolute-value detectors opted for independent modules for each function stage. The sign bit operates bit inversion and increment-by-one to select whether the input is reconstructed or forwarded. This modular partition clearly decouples magnitude computation and sign detection, which gives a clear route for circuit design.

Ge et al. addressed the practical problem that additional logic levels and transistor usages extend signal propagation and critical path delay [3]. In this study, the mirror carry adder architecture is implemented in LTspice for further parameter sensitivity analysis. But to run simulation tests, each input bit is driven by a two-stage inverter buffer, resulting in eight additional inverter use beside the core six inverters. Furthermore, a $32C_{g1}$ capacitive load is connected at the output node to simulate realistic driving environment and provide a consistent basis for measuring propagation delay and energy.

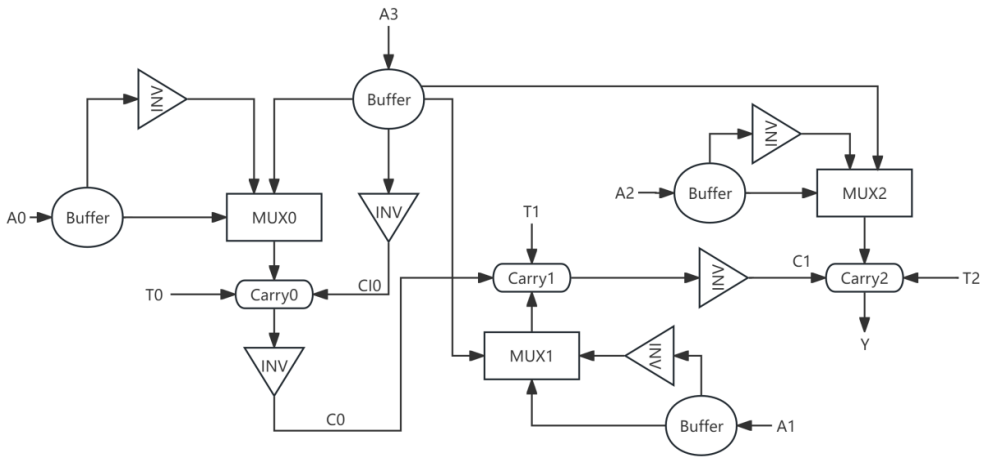

Figure 1. Overall Circuit Structure in Blocks (Picture credit: Original)

The overall circuit architecture is shown in Figure 1. Its transistor-level specification in LTspice is presented in Figures 2-6, including the input buffers, inverters, multiplexers, mirror-adder carry modules, and interstage carry inverters. In these schematics, the buffered input signals are denoted as BfdA0, BfdA1, BfdA2 and BfdA3; CI0 is the initial carry input signal applied to the first mirror-adder carry unit, C0_RAW and C1_RAW are C0 and C1 signals before inversions, C0 denotes the carry signal generated by the first mirror-adder carry unit and C1 is the carry signal propagated from the first carry stage to the subsequent arithmetic stage; Y stands for the final detector output. For the block names, SC13 and SC14 are the inverters before C0 and C1; SC1, SC3, SC6 and SC9 are the buffer inverters.

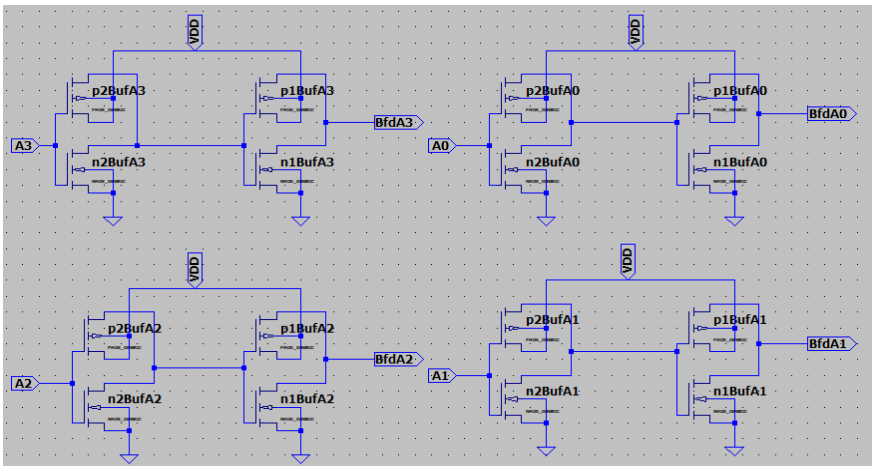

Figure 2. MOS-Level Schematic of the 4-Bit Input Buffer Module (Picture credit: Original)

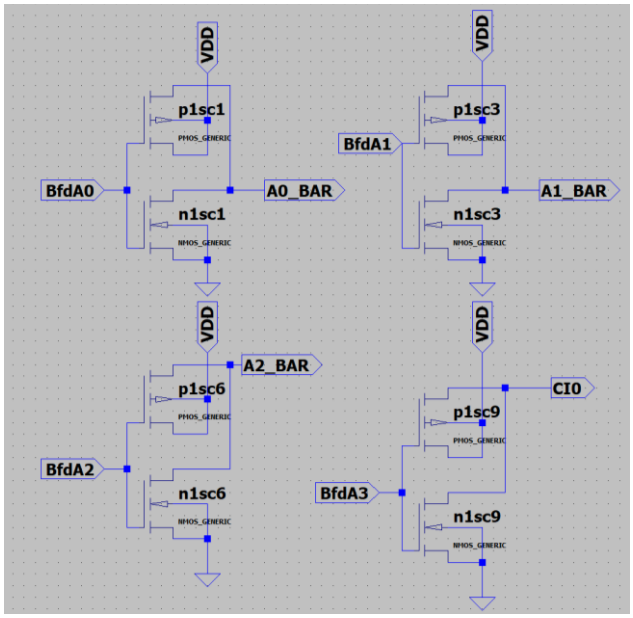

Figure 3. MOS-Level Schematics of the Data and Initial-Carry Inverters (Picture credit: Original)

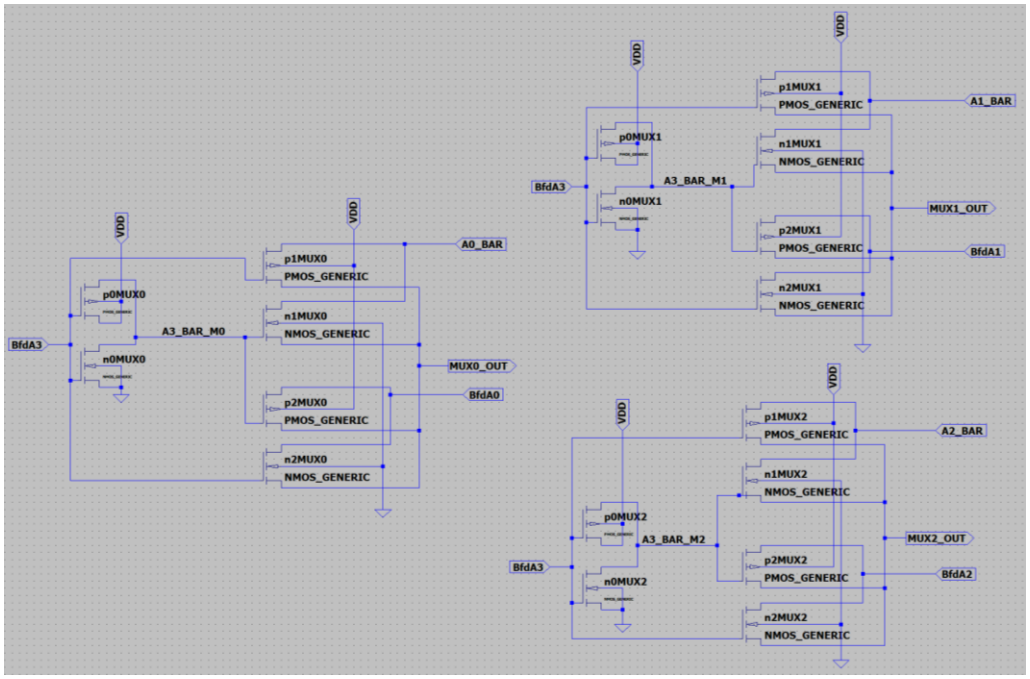

Figure 4. MOS-Level Schematics of the Three Multiplexer Modules (Picture credit: Original)

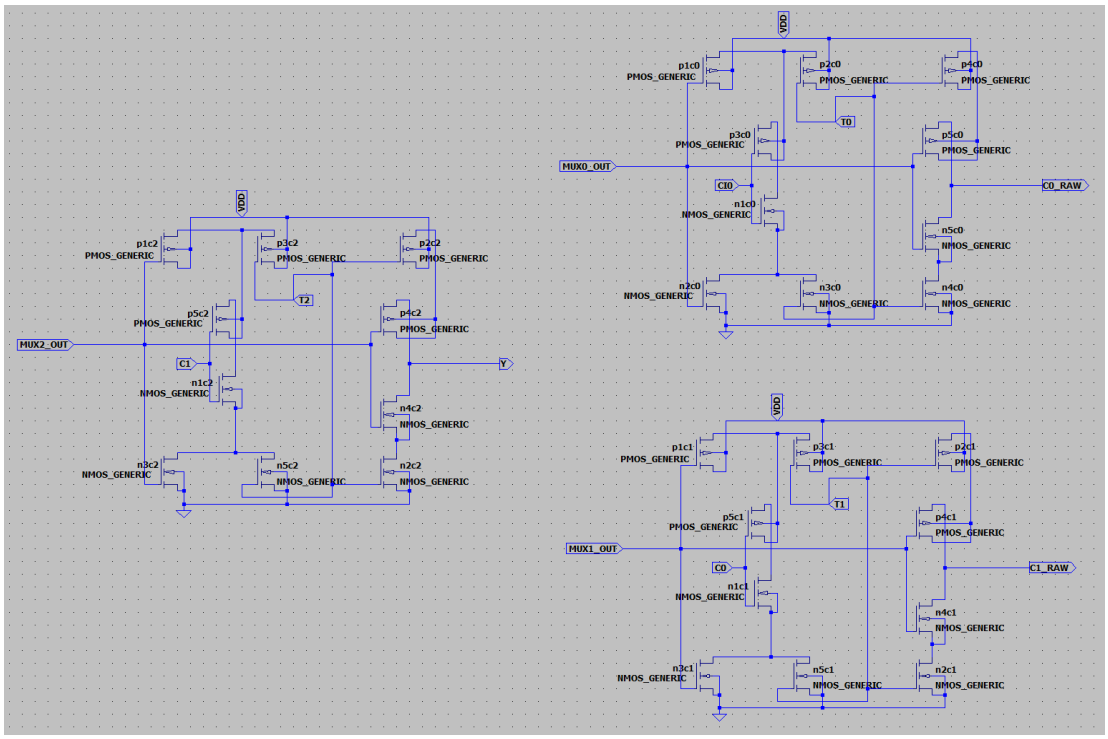

Figure 5. MOS-Level Schematics of the Three Mirror-Adder Carry Modules (Picture credit: Original)

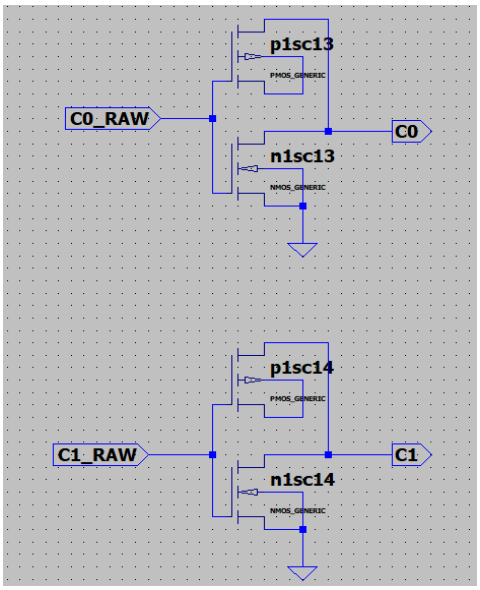

Figure 6. MOS-Level Schematics of the Interstage Carry Inverters (Picture credit: Original)

In this study, the optimized architecture proposed by Ge et al. is selected as the reference structure for transistor-level investigation. Instead of modifying the circuit topology, this work focuses on analyzing the influence of key parameters, including transistor sizing and supply voltage variation, on delay and energy performance. All simulations are conducted using LTspice with identical device models and simulation settings. The propagation delay and energy consumption obtained from the reference structure are used as baseline metrics for subsequent optimization and sensitivity analysis, ensuring that the observed performance variations are mainly attributed to parameter changes.

2.3. Design Parameters and Evaluation Metrics

The performance of CMOS absolute-value detectors is influenced by both logical architecture and transistor-level parameters. In this study, transistor sizing and supply voltage are selected as the main design variables for evaluating their effects on delay–energy characteristics. Transistor-level

parameters directly influence the delay and energy characteristics of CMOS arithmetic circuits, making device dimensions and operating conditions important design variables [8].

The supply voltage V_{DD} directly affects transistor switching behavior and circuit efficiency. Supply-voltage scaling provides an effective means of reducing CMOS energy consumption, although operation at reduced V_{DD} increases timing sensitivity and places tighter requirements on critical-path delay [9]. Dynamic energy consumption increases with voltage according to:

$$E_{dynamic} = C_{load}V_{DD}^2 \tag{3}$$

where Cload represents the effective switching capacitance. Therefore, voltage scaling requires a balance between energy reduction and acceptable circuit speed.

Propagation delay and energy-related metrics are widely used together to characterize the performance of CMOS arithmetic circuits because improvements in speed may be accompanied by increased energy cost [10]. Propagation delay reflects the response time of the output signal and is determined mainly by the critical path, which can be expressed as:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \tag{4}$$

where t_{pHL} and t_{pLH} represent high-to-low and low-to-high transition delays, respectively. Energy consumption is mainly associated with capacitive charging and discharging during switching operations. Since delay reduction often leads to increased energy consumption, this study analyzes the delay–energy trade-off rather than optimizing a single parameter independently. The obtained evaluation framework provides the basis for subsequent LTspice simulations and parameter sensitivity analysis.

3. Simulation Experiment Design

3.1. Reference Circuit and LTspice Simulation Conditions

To enable controlled parametric comparisons, a unified LTspice simulation environment is established using a common set of device models, loading conditions, and measurement procedures. The 4-bit CMOS absolute-value detector architecture described in 2.2 is used as the reference circuit, whose structure remains unchanged through the whole experiment. This experiment took transistor sizing and supply voltage as the principal variables.

The reference circuit has a 4-bit two's complement input, and its voltage ranges from -7 to +7. As was mentioned in section 2.2, each input signal is driven by a two-inverter buffer while the output is connected to a normalized capacitive load of $32C_{g1}$. C_{g1} denotes the input gate capacitance of the unit inverter. A unit inverter is defined by $L_p = L_n = 100$nm, and $W_p = 300$nm, $W_n = 200$nm. A nominal supply voltage of $V_{DD} = 1$V is selected for reference simulation, during which V_{DD} is tweaked due to the delay-energy sizing explorations. The principal LTspice simulation conditions are summarized in Table 1.

Table 1. LTspice Simulation Conditions

Parameter	Value
Input	4-bit two's complement
Input Range	-7 to +7
Nominal V_{DD}	1V
Unit PMOS	300nm
Unit NMOS	200nm
Channel length	100nm
Input driver	Two cascaded unit inverters
Output load	$32C_{g1}$

Propagation delay measurement starts at the buffed input signals and ends at the detector output Y. By evaluating the relevant input transitions, the condition yielding the maximum propagation delay is marked as the practical worst-case delay. This worst-case input pattern appears in multiple subsequent sections of this thesis. This experiment then examines simulated energy consumption during the specified switching operations. The device models, loading and driving conditions, measurement definitions of transient cases are fixed across all experiment groups so that variations among scanned parameters give rise to the measured gaps in circuit performance.

3.2. Group A: Reference circuit evaluation based on the selected optimized architecture

Group A establishes the reference performance of the selected circuit under the baseline LTspice conditions defined in Section 3.1. The purpose of this group is to verify the functional correctness of the 4-bit absolute-value detector and to obtain its initial propagation-delay and energy characteristics before any transistor-sizing or supply-voltage optimization is introduced.

Functional verification is first performed using the specified 4-bit two's-complement input combinations to confirm the correct absolute-value detection operation. Following functional verification, propagation delay is evaluated using the worst-case input pattern defined in Section 3.1, and the relevant energy consumption is measured under the same circuit and loading conditions. No transistor-sizing optimization is performed in Group A.

The resulting propagation delay and energy consumption are denoted as D_{ref} and E_{ref}, respectively, and are used as the baseline for comparison with Groups B and C.

3.3. Group B: Delay optimization by transistor sizing adjustment to determine the minimum-delay operating point.

The purpose of Group B is to evaluate the effect of transistor sizing on the propagation delay of the reference circuit and identify the minimum-delay operating condition. This stage does not change the V_{DD}, but adjusts transistor dimensions to enhance total circuit drive strength.

As discussed in section 2.3, transistor sizing produces drive strength and capacitive loading, affecting delay data. According to the critical path information Group A addresses, Group B optimizes the transistors constructing the dominant delay path. This experiment group also adopted the sizing principle guided by logical effort analysis, allowing transistor dimensions to be adjusted by stage loading and electrical effort [7].

After optimizing the dominant delay path, the circuit is simulated in LTspice with unchanged input patterns and loading conditions. Group B extracts a new practical worst case delay and define the attained minimum value as D_{min}. This optimized data set is employed as a reference point and quantitatively evaluates the relationship between sizing and delay, paving the way for Group C.

3.4. Group C: Energy Optimization under a Delay Constraint to Identify an Energy-Efficient Operating Region

Energy reduction in CMOS logic can be cast as a constrained optimization problem, where sizing and voltage scaling are jointly considered while maintaining specified simulation requirements [11]. Group C uses the obtained D_{min} from Group B and places emphasis on energy reduction. This experiment group captures the delay-energy trade-off by sweeping the operating point delay and energy per operation. These data are concluded into the delay-energy curve and used to identify operating point with minimum energy consumption, or viable operating region.

The energy consumption is calculated by integrating the instantaneous power supplied by the V_{DD} source during the transient simulation. The energy is calculated as:

$$E = \int_{t0}^{t1} -V_{DD} I_{DD}(t) dt \tag{5}$$

A delay limit of $1.4D_{min}$ is employed as an engineering timing constraint, which is a design constraint rather than a universal optimal delay-energy ratio. This limit relaxes the minimum delay condition for 40% and sets the permissible timing budget for energy reduction. Its plausibility and practical effect are evaluated from the parametric results in Chapter 4. The D_{min} Group B yielded is used as the timing baseline for energy refinement, Group C progressively reduces supply voltage from the nominal 1V. To offset the degradation brought by this, transistor dimensions are in turn adjusted at each voltage level.

For each V_{DD} and sizing configuration, LTspice transient simulations carries over the defined input conditions and loading environment in section 3.1. The worst-case propagation delay and energy consumption values for each setup. This experiment compiles the data points under different voltage and sizing combinations and plots their curve via Python. The feasible operating region is defined by the delay constraint:

$$D\ (V_{DD}, W)\ \leq\ 1.4D_{min} \tag{6}$$

W stands for transistor widths. Among the simulated configurations, the energy-efficient operating point is the one with the minimum measured energy consumption. This approach enforces the practical region with low energy instead of any configurable voltage set points.

For each configuration, delay and energy are evaluated simultaneously rather than inferring energy improvement from V_{DD} reduction alone. The resulting data are analyzed in Chapter 4 to characterize parameter sensitivity and the constrained delay–energy trade-off.

4. Sensitivity Analysis and Discussion of Simulation Results

4.1. Comparative Analysis of Results

The three experimental groups illustrate the transition from reference-circuit characterization to delay optimization and finally to energy-oriented optimization. The principal results are summarized in Table 2.

Table 2. Comparison of the Three Experimental Groups

Group	V_{DD}(V)	Worst-Case Delay (ps)	Energy (pJ)	Main Objective
A	1.000	148.262	13.663	Reference evaluation
B	1.000	85.560	16.950	Minimum delay
C	0.828	119.761	8.769	Minimum energy under delay constraint

Group A represents the unmodified reference condition at V_{DD} =1V, with a worst-case propagation delay of 148.262 ps and an energy consumption of 13.663 pJ.

This paper defines the worst case of Group A LTspice delay transition is Case09. Figures 7 and 8 visualizes the propagation delay, which is evaluated between the 50% V_{DD} of the buffered input BfdA0 and the global output Y. Those crossings are generated by an LTspice function named ‘Place Cursor on Active Trace’. They marked approximately 276.013 ns and 276.162 ns for both V(BfdA0) and V(Y) operates at around 0.50 V. The LTspice meas evaluation gives a worst-case propagation delay of 148.262 ps, which is adopted as the reference delay D_{ref} for Group A.

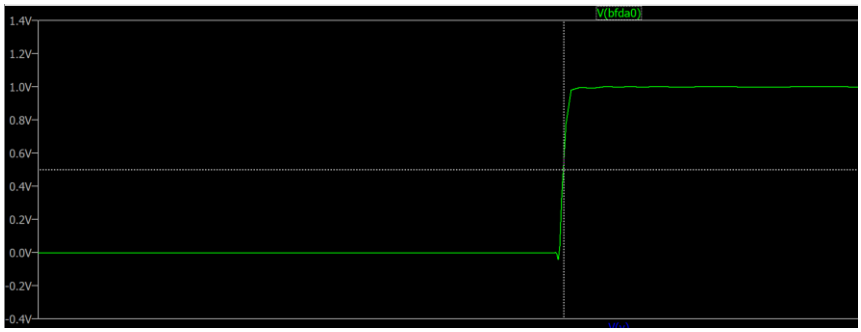

Figure 7. Transient Response of the Buffered Input Signal BfdA0 for the Group A Worst-Case Transition. (Picture credit: Original)

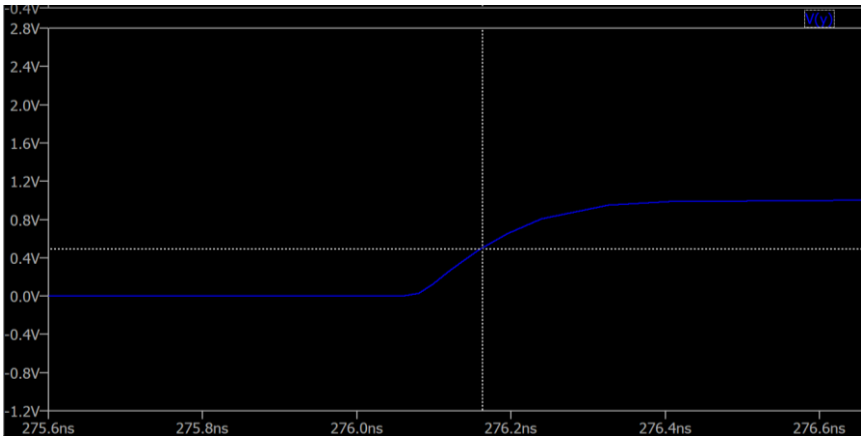

Figure 8. Transient Response of the Detector Output Y for the Group A Worst-Case Transition. (Picture credit: Original)

Table 3 is the optimization log of transistor sizing, tracing the sizing alternations for the width of PMOS and NMOS transistors. After these dimension changes, the minimum delay D_{min} is reduced to 85.56 ps, while the energy rose to 16.950 pJ. Their relation to Group A is a 42.3% reduction in delay and 24.1% rise in energy, confirming that delay minimization alone does not effectively save energy.

Table 3. Summary of sequential transistor-sizing optimization results.

Optimized device	Optimization Target	Final Dimension	Effect
C2	Output driving stage	Wp =2.4μm, Wn= 1.6μm	Reduced output transition
SC14	Critical carry path	Wp =900nm, Wn= 600nm	Improved critical path delay
Mp1c1 / Mp5c1	Pull-up path	Wp =600nm, Wn= 600nm (unchanged)	Larger sizing increased delay
Mn1sc13	Internal carry path	300nm	Delay improvement saturated after 300nm
Mn1sc6	Internal Path	300nm	Further sizing improvements are negligible

Group C started V_{DD} adjustment with the output driving stage (C2). At V_{DD}=0.850 V, the C2 transistor configuration of W_p =2.4μm, W_n= 1.6μm delivers 117.455 ps delay and 9.611 pJ energy, while further adjustments on C2 transistors exceeds the delay results. Group C then concentrates on the mirror-adder carry path. At V_{DD} = 0.845V, transistors named Mp4c0 and Mp5c0 go through 1.00 μm to 600 nm widths and delay decreases from 118.574 ps to 116.102 ps in this process. At last, Group C changes the widths of the multiplexer control transistor Mn1MUX0 from 1.00 μm to 600 nm, and the delay changed from 118.574 ps to 116.102 ps. The final energy-efficient operating point of Group C converges to V_{DD} = 0.828 V, the worst-case delay is 119.761 ps which does not exceed the adopted 1.4D_{min} (119.78 ps) constraint. Compared with Group B configuration. Group C maintains acceptable circuit timing performance and reduces energy consumption from 16.950 pJ to 8.769 pJ, roughly 48.3% reduction.

Figures 9 and 10 are the final operating waveforms of Group B and Group C. The waveform simulation reflects that the timing consequence of moving from delay-oriented transistor sizing to constrained energy optimization. Group B realizes the highest circuit speed at the cost of energy, Group C properly regulates this sacrifice to narrow down the tuning range.

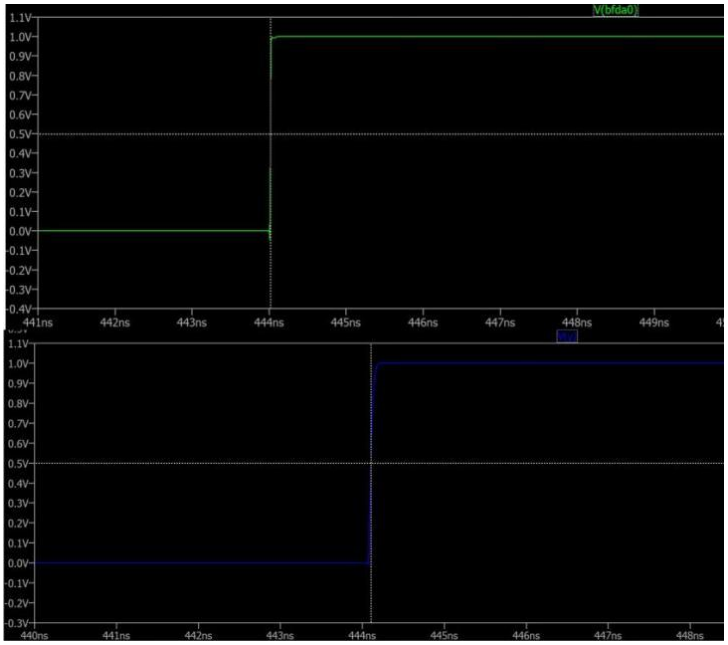

Figure 9. Critical-Transition Waveforms under the Final Operating Condition of Group B Minimum-Delay Condition at V_{DD}=1.0V (Picture credit: Original)

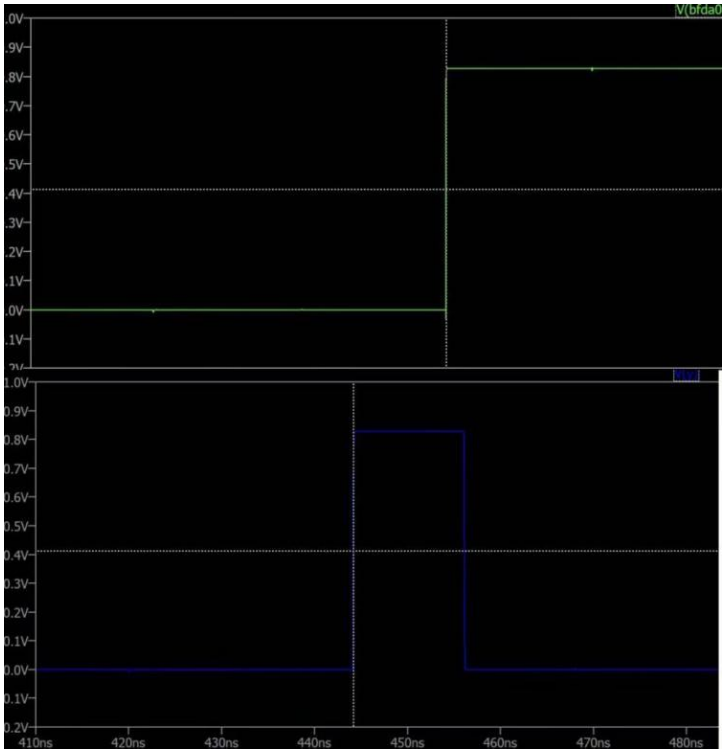

Figure 10. Critical-Transition Waveforms under the Final Operating Condition of Group C Energy-Optimized Condition at V_{DD}=0.828V. (Picture credit: Original)

4.2. Impact of Parameter Changes on Delay and Energy Consumption

Figures 11 and 12 are the Python plots of section 4.1 experimental results, the horizontal axis are sizing scales and the vertical axis are the change rates of delay and energy. These data are retrieved from the transistor-sizing sweep results in Group B. For each device, the curve begins at Group A

sizing baseline and the trend depicts the optimization outcomes of Group B and C. Taken together, C2 possesses the strongest sizing sensitivity, which yields around 32% delay improvement but also induces the highest energy penalty nearly 29%. SC14 reached additional delay improvement close to 10%, yet energy consumption increases only to a modest extent. Several curves even show diminishing enhancement. CMOS design principle entails joint evaluation of delay and energy metrics in preference to device sizing alone [12].

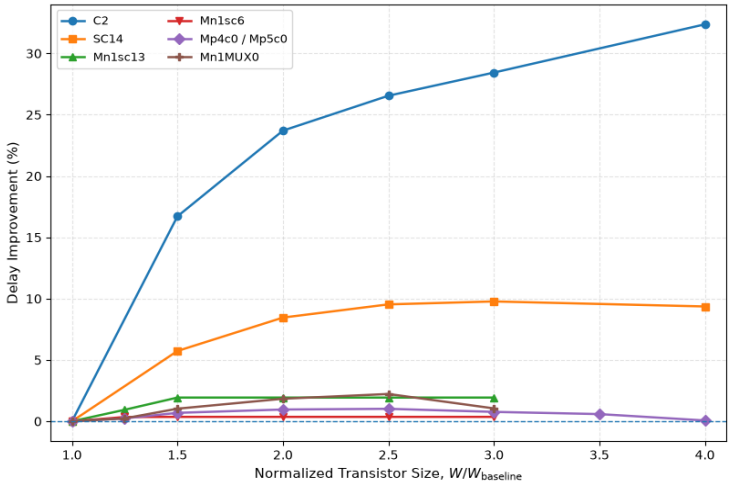

Figure 11. Delay sensitivity of selected critical-path transistors to sizing variations. (Picture credit: Original)

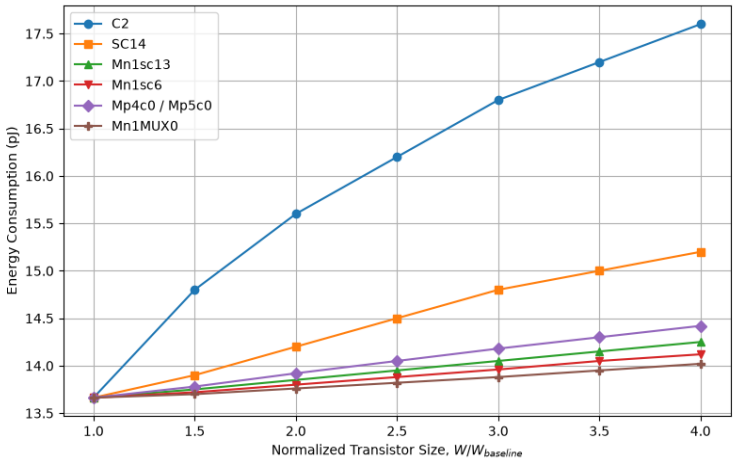

Figure 12. Energy sensitivity of selected critical-path transistors to sizing variations. (Picture credit: Original)

One operating point in Group C is in the vicinity of V_{DD}=0.842V, it delivers 119.778 ps delay and an 9.304 pJ, with notable savings on energy. Further transistor sizing brought voltage down to 0.828 V while respecting the delay constraint, with final energy value converges to 8.769 pJ.

These observations highlight that downsizing transistors does not always reduce total energy under a delay constraint. Driving capability degrades as the cost of parasitic capacitance decrease, so the circuit necessitates additional voltage compensation to comply with the intended timing limits. Circuit level observations from low-voltage CMOS work show that voltage tuning and timing margin budgeting should be treated dependently, near the minimum feasible supply voltage in particular [13].

4.3. Parameter Sensitivity Analysis and Discussion

Propagation delay and energy consumption especially sensitive to device sizing on the dominant signal path. The Group C results underlines that the delay-energy trade-off is shaped by the interplay

of transistor sizing and supply voltage. Chapter 4 indicates that parameter sensitivity analysis are essential for identifying low-energy operating regions.

Different parameters influence circuit characteristics through different mechanisms: transistor sizing primarily shapes driving strength and delay response, while supply voltage tuning exerts a strong influence over total energy draw, alongside inherent timing penalty trade-offs. Thus, optimized circuit cannot be attained through isolated parameter tuning, requiring comprehensive assessment of parameter interplay. Its necessity has been underscored by Group C result. This experiment group retains D_{min} as the fixed timing reference and coordinates sizing with V_{DD}. This co-tuned setup yields 8.769 pJ at 119.761 ps. Parameter-sensitivity trends might be leveraged to move the circuit toward far lower-energy operating states, while respecting the selected timing bounds.

These derived findings support the rationality for applying the $1.4D_{min}$ constraint to the investigated circuit. This selected relaxation factor prevents undue performance degradation and secures energy-centric optimization within sufficient time margin. While the precise optimal optimal relaxation factor varies with circuit architecture and design priorities, the measurement confirms that 1.4 D_{min} forms a viable operating boundary to trade off energy savings against timing constraint for the present design.

5. Conclusion

This study explored the delay-energy trade-off and parameter sensitivity of a CMOS 4-bit absolute-value computation circuit with threshold detection. The circuit function was tested through LTspice transistor-level simulation. Starting from the three-stage carry-adder structure, three experimental groups were designed to distinguish baseline performance, latency-prioritized sizing strategies and bounded energy optimization.

The circuit Group A constructed recorded a peak propagation delay of 148.262 ps and a 13.663 pJ energy. Group B reduced the delay to 85.560 ps by sizing transistors, although the energy consumption increased to 16.950pJ. The LTspice sweep under different sets of sizing conditions further revealed that devices on the dominant signal path present markedly different delay-response sensitivities. The most dominant device parameter delivering a performance gains of roughly 32%. These results confirm that uniform transistor upsizing yields suboptimal efficiency, and transistor sizing should prioritize delay-critical stages instead.

Group C conducted energy-centric optimization using the minimum delay Group B simulated as a fixed timing reference. Applying the $1.4D_{min}$ timing constraint, the optimal design operating point is attained at 0.828 V supply, giving a worst case delay of 119.761 ps and 8.769 pJ energy consumption. This delivers a 48.3% reduction over the minimum-delay counterpart, while fully complying with the imposed timing constraint. The results verified that combined tuning of device dimensions and supply voltage is necessary. Although the adopted $1.4D_{min}$ constraint provides a useful operating boundary for this circuit, future investigations should examine extended delay constraints as well as process, voltage, and temperature variations to validate the method's generality and robustness.

References

[1] S. S. Sriram Sundar and G. Mahendran, "CMOS full adder cells based on modified full swing restored complementary pass transistor logic for energy efficient high speed arithmetic applications," Integration, vol. 95, Art. no. 102132, 2024, doi: 10.1016/j.vlsi.2023.102132.

[2] A. Burman, J. Solé-Casals, and S. E. Lew, "Robust and memory-less median estimation for real-time spike detection," PLoS ONE, vol. 19, no. 11, Art. no. e0308125, 2024, doi: 10.1371/journal.pone.0308125.

[3] J. Ge, J. Yang, and C. Zhao, "A 1.17ns FO4(1V) low energy cost 4-bit absolute-value detector," in Proc. 2021 International Conference on Electronic Information Engineering and Computer Science (EIECS), 2021, pp. 985–993, doi: 10.1109/EIECS53707.2021.9588022.

[4] X. Fan, H. Liu, H. Li, S. Lu, and J. Han, "Design of light-weight timing error detection and correction circuits for energy-efficient near-threshold voltage operation," Electronics, vol. 11, no. 18, Art. no. 2879, 2022, doi: 10.3390/electronics11182879.

[5] U. Sharma and M. Jhamb, “A novel design of voltage and temperature resilient 9-T domino logic XOR/XNOR cell,” Circuits, Systems, and Signal Processing, vol. 41, 2022, pp. 6314-6332, doi: 10.1007/s00034-022-02085-5.

[6] S. S. Dash, “Optimal design of voltage reference circuit and ring oscillator circuit using multiobjective differential evolution algorithm,” Journal of Electrical and Computer Engineering, vol. 2023, Art. no. 7621594, 2023, doi: 10.1155/2023/7621594.

[7] K. Singh, A. Jain, A. Mittal, V. Yadav, A. A. Singh, A. K. Jain, and M. Gupta, “Optimum transistor sizing of CMOS logic circuits using logical effort theory and evolutionary algorithms,” Integration, vol. 60, pp. 25–38, 2018, doi: 10.1016/j.vlsi.2017.08.003.

[8] O. Anjaneyulu and C. V. Krishna Reddy, “A novel design of full adder cell for VLSI applications,” International Journal of Electronics, vol. 110, no. 4, pp. 670–685, 2023, doi: 10.1080/00207217.2022.2059819.

[9] J. Liu, K. Wang, J. Yin, X. Zhao, Z. Li, H. Zhao, and S. Qiao, “A dynamic voltage scaling circuit design based on critical path replica and time warning techniques,” IEICE Electronics Express, vol. 21, no. 2, Art. no. 20220520, 2024, doi: 10.1587/elex.20.20220520.

[10] M. M. Basha, S. Gundala, and S. I. Khan, “Design of energy and EDP efficient 1-bit full subtractor based divider circuits for computing systems,” International Journal of System of Systems Engineering, vol. 11, nos. 3–4, pp. 257–267, 2021, doi: 10.1504/IJSSE.2021.121462.

[11] A. Kabbani, “Logical effort based dynamic power estimation and optimization of static CMOS circuits,” Integration, vol. 43, no. 3, pp. 279–288, 2010, doi: 10.1016/j.vlsi.2010.02.002.

[12] S. S. Subramanian et al., “Low Power CMOS Full Adder Cells based on Alternative Logic for High-Speed Arithmetic Applications,” Informacije MIDEM, vol. 54, no. 3, pp. 187–200, 2024, doi: 10.33180/InfMIDEM2024.303.

[13] R.-Z. Yu, Z.-H. Li, X. Deng, and Z.-L. Liu, “Negative Design Margin Realization through Deep Path Activity Detection Combined with Dynamic Voltage Scaling in a 55 nm Near-Threshold 32-Bit Microcontroller,” Sensors, vol. 23, no. 17, Art. no. 7498, 2023, doi: 10.3390/s23177498.