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Performance Trade-Off Analysis of Low-Power Wearable ECG Analog Front Ends

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Abstract. Wearable electrocardiogram (ECG) devices need analog front-end (AFE) circuits that can detect microvolt-to-millivolt cardiac signals continuously for extended periods with very small batteries or harvested energy. The first amplification stage strongly influences total input-referred noise and therefore requires careful allocation of the power budget. This paper studies the engineering trade-off between input-referred noise and power consumption in low-power operational-amplifier-based ECG AFEs. This comparative literature review examines peer-reviewed designs published from 2015 to 2026 and draws on established work on chopper stabilization, auto-zero techniques, common-mode interference and wearable biosensing. The comparison includes power, integrated input-referred noise, gain, bandwidth, common-mode rejection ratio, input impedance and noise efficiency where reported. The results show that there is no single universally optimal AFE; the lowest-power designs reviewed here accept higher noise, and sub-microvolt noise generally requires microwatt-level power or more advanced circuit techniques. Chopper stabilization, current reuse, weak-inversion biasing, capacitive coupling and digitally assisted offset cancellation can be used to shift this trade-off, but each has its own disadvantages, such as ripple, reduced input impedance, bandwidth limitations, area or circuit complexity. Therefore, future wearable ECG AFEs should focus on adaptive, application-specific biasing and standardized multi-metric benchmarking rather than solely reducing power consumption or noise.

Keywords: Wearable ECG; Analog Front-End; Operational Amplifier; Low Power; Input-Referred Noise.

1. Introduction

Wearable health-monitoring systems have shifted physiological measurements from short-term clinical observations to long-term, daily monitoring. Among the signals acquired by wearable health devices, electrocardiograms are particularly useful because they record the electrical activity of the heart. Extended ECG monitoring can identify intermittent rhythm disturbances that may not appear during a brief clinical recording, and wearable devices are available for 24-hour monitoring outside the hospital. Therefore, the research focus of wearable biosensor systems has been to achieve unobtrusive sensing, low power consumption, reliable signal acquisition and sufficient processing capabilities [1,2]. A recent review specifically on ECG analog front-ends has also identified low power consumption, low noise, common-mode interference rejection and high input impedance as the main design requirements for portable ECG acquisition [1].

The analog front-end is the interface between the electrodes on the body and the digital processing unit. Figure 1 shows the signal path from skin electrodes through analog amplification and filtering to an analog-to-digital converter (ADC) and digital processing. The electrodes detect a small differential biopotential, but the desired ECG waveform is accompanied by electrode DC offset, motion artifacts, power-line interference, thermal noise and low-frequency flicker noise. Wearable ECG amplitudes are generally in the range of tens of microvolts to a few millivolts, and unwanted disturbances can be as large as or much larger than the signal itself [1,3]. Power-line interference is particularly severe because capacitive coupling from the electrical environment can manifest as a large common-mode signal; thus, a high common-mode rejection ratio (CMRR), balanced electrode interfaces and careful front-end design are required [4]. Dynamic wearable measurements also introduce artifacts due to motion, altered electrode impedance, respiration and contact instability [5].

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Wearable devices also have a limited energy budget. Continuous monitoring requires long operating times from a small battery or a harvested energy supply. These goals are in direct conflict with low-noise analog design. To reduce the input-referred thermal noise of a MOS input stage, a relatively large transconductance is generally required; this larger transconductance can be achieved by increasing the bias current or using circuit techniques that enhance transconductance efficiency. Lowering supply voltage reduces power, but it also reduces voltage headroom and can make high-gain, high-linearity analog design more difficult. Therefore, the low-noise amplifier or instrumentation amplifier stage is often one of the most critical design points in an ECG AFE [1,6,7].

Low-frequency ECG acquisition also makes flicker noise important. Chopper stabilization reduces offset and low-frequency noise by modulation, while auto-zeroing samples and subtracts the amplifier error [8]. Chopper-stabilized amplifiers are now commonly used in biomedical front-ends because they can reduce 1/f noise without a continuously high bias current. Switching also introduces ripple, spikes, charge injection, aliasing and a possible reduction in input impedance. Therefore, recent ECG front-ends have combined chopping with capacitive coupling, DC-servo loops (DSLs), passive ripple filters, programmable gain, digitally assisted offset cancellation or positive-feedback impedance boosting [3,6,9,10].

Published designs demonstrate that the appropriate power-noise trade-off depends on the application. Harpe et al. reported a fully integrated 3 nW signal-acquisition IC for ECG recording, but its total input noise is 27 μVrms [11]. Kosari et al. showed a 68 nW ECG AFE with 2.8 μVrms input-referred noise and a tunable 31–52 dB gain [12]. At higher power, Song et al. obtained 0.34 μVrms from a chopper-stabilized fetal-ECG amplifier system consuming 1.56 μW [6], and Yang et al. reported 0.39 μVrms for a 4 μW long-term ECG AFE [9]. The above examples show that power alone cannot determine the best architecture; rather, the required trade-off depends on whether the goal is simple heart-rate monitoring, morphological analysis that preserves P waves, fetal ECG, batteryless sensing, or a more general diagnostic-grade wearable system.

Therefore, the research question of this paper is: How should designers balance noise and power in low-power operational-amplifier-based wearable ECG AFEs, and which circuit techniques can improve this balance most effectively? This paper addresses the question through a comparative literature study with three contributions. First, it organizes the main noise and power mechanisms in a general engineering framework. Second, it compares representative published designs based on reported power, noise, bandwidth, gain, CMRR and other indicators, and explicitly identifies differences in test conditions. Third, it converts the comparison into practical design directions for wearable ECG devices. Individual papers usually optimize a specific architecture, while broad reviews cover many circuit types. This focused comparison clarifies why the lowest-power design may not meet the signal-quality requirements of a particular wearable ECG application.

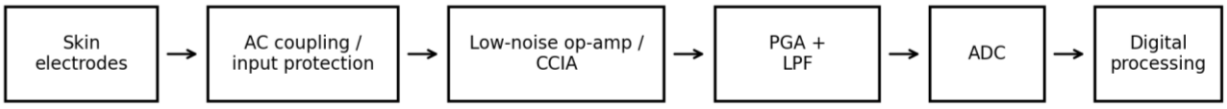

Fig. 1 Simplified wearable ECG analog front-end signal chain, synthesized from [1,3,6,7,9,10]. (Picture credit: Original)

CCIA: capacitively coupled instrumentation amplifier; PGA: programmable gain amplifier; LPF: low-pass filter; ADC: analog-to-digital converter.

2. Methodology and Analytical Framework

This study uses a comparative literature-review method. The source set includes foundational circuit papers and representative wearable or biopotential AFE implementations. Priority was given to peer-reviewed journal publications that reported numerical results for power consumption and input-referred noise, as these two quantities are the primary comparison metrics. The selected implementation papers include a low-voltage current-reuse chopper amplifier for fetal ECG [6], a 0.5

V chopper-stabilized instrumentation amplifier [7], a 3 nW integrated acquisition IC [11], a 68 nW ECG AFE [12], a 4 μW long-term ECG AFE [9], a programmable 48 μW ECG AFE [10], and a 2026 wearable ECG AFE using a dedicated chopper-spike filter [3]. Broader review and interference papers are used to define the measurement problem and interpret the design trade-offs [1,4,5,8].

The comparison considers both power consumption and ECG signal-quality metrics, as summarized in Table 1. Input-referred noise is the equivalent noise at the amplifier input that would produce the observed output noise. Integrated noise should always be considered in conjunction with the integration bandwidth; a noise value measured in the range of 0.7–182 Hz is not the same as one integrated from 0.5 Hz to 1 kHz. CMRR is the rejection of common-mode interference, and input impedance determines the impact of electrode impedance and dry-contact conditions on the signal. Gain and bandwidth determine whether the desired ECG shape can be amplified without clipping or filtering out clinically significant features. The noise efficiency factor (NEF) and power efficiency factor (PEF) are normalized efficiency indicators, but they are only included if the original authors have reported them, as different definitions and system scopes may lead to misleading comparisons.

Power is calculated from the supply voltage and current when a source reports current instead of power. For instance, the 2026 Sadeghi–Yavari AFE draws 2.44 μA at 1.8 V, corresponding to approximately 4.39 μW [3]. The relationship is:

$$P = V_{\mathrm{DD}} \times I_{\mathrm{total}} \tag{1}$$

For noise, the integrated input-referred root-mean-square value is obtained by integrating the input-referred noise power spectral density over the signal bandwidth:

$$v_{\mathrm{n,rms}} = \sqrt{\int_{f_{\mathrm{L}}}^{f_{\mathrm{H}}} S_v(f)\,\mathrm{d}f} \tag{2}$$

At the transistor level, a useful first-order relationship for the thermal component of MOS input-stage noise is that the input-referred noise spectral density decreases as transconductance increases. A simplified single-transistor expression is:

$$e_{\mathrm{n,thermal}}^2 \approx \frac{4kT\gamma}{g_m} \tag{3}$$

This relationship illustrates the power-noise trade-off: raising the bias current generally boosts transconductance and lowers thermal noise, but at the cost of higher power consumption. Operating MOS devices in weak inversion can enhance the transconductance-to-current efficiency, and current-reuse or inverter-based structures can achieve a higher effective transconductance with the same current. Chopping mainly reduces low-frequency flicker noise and offset without altering the thermal-noise relationship [6-8]. The signal-to-noise ratio (SNR), expressed in decibels, can be written as:

$$\mathrm{SNR} = 20\,\log_{10}\left(\frac{V_{\mathrm{signal,rms}}}{V_{\mathrm{noise,rms}}}\right) \tag{4}$$

The analysis does not assume that the plotted designs are perfectly controlled benchmarks. Process technology, supply voltage, bandwidth, channel count, measured-versus-simulated status, inclusion of ADCs, electrode conditions, and offset-cancellation circuits all differ among the papers. Therefore, Figure 2 and Table 3 are engineering comparisons of the reported operating points, not claims that one paper is superior to another. This distinction matters because the most energy-efficient design for heart-rate extraction may not preserve the low-amplitude ECG morphology as well as a design that allocates more power to the first amplifier stage.

Table 1. Metrics used to evaluate wearable ECG AFEs

Metric	Engineering meaning	Why it matters in wearable ECG
Power consumption	Electrical energy used per unit time	Controls battery life, self-powered feasibility, and heat
Input-referred noise	Equivalent amplifier noise referred to the electrodes	Determines whether small ECG features remain visible
Bandwidth	Frequency range passed by the AFE	Sets both useful signal content and integrated noise
CMRR	Rejection of common-mode inputs	Reduces power-line and environmental interference
Input impedance	Electrical loading presented to electrodes	Critical with dry/high-impedance wearable electrodes
Gain / dynamic range	Amount of amplification before conversion	Must amplify ECG without saturating from offset or artifacts
NEF / PEF	Normalized noise–power efficiency indicators	Useful for comparing amplifier efficiency when definitions align

3. Noise-Reduction and Low-Power Techniques

3.1. Chopper Stabilization and Auto-Zero Techniques

Chopper stabilization is widely used to reduce noise in low-frequency biomedical amplifiers. In the ideal case, the input signal is first modulated at a higher chopping frequency before amplification. The amplifier's offset and 1/f noise are introduced after the input modulator. A second modulation stage returns the desired signal to baseband while shifting these low-frequency errors to the chopping frequency and its harmonics, where filtering can suppress them. Enz and Temes have presented the classic analysis of auto-zeroing, correlated double sampling and chopper stabilization, showing that these methods reduce offset and low-frequency noise by using time-varying signal processing rather than increasing the analog bias current [8].

Chopping is attractive for ECG acquisition because low-frequency ECG signals are vulnerable to flicker noise. Song et al. used a current-reuse chopper-stabilized amplifier to report a noise of 0.34 μVrms over 0.7–182 Hz, and the entire amplifier plus power-management circuitry consumed 1.56 μW [6]. Yang et al. later combined a chopper amplifier and passive noise filtering, along with pulse-width modulation-based offset cancellation, to achieve 0.39 μVrms and 4 μW, and showed visible P waves in a long-term ECG prototype [9]. These designs demonstrate sub-microvolt integrated noise at microwatt-level power using chopping and supporting circuit techniques.

Chopping does not solve all the problems. Switching generates spikes, ripple and charge-injection artifacts, and the switched input capacitance can reduce the effective input impedance at the electrode interface. Therefore, recent research addresses both the advantages and disadvantages of chopping. Han et al. used independent biasing to stabilize the operating point and reduce chopping glitches in a programmable AFE [10]. Sadeghi and Yavari proposed a dedicated chopper spike filter in 2026, together with positive-feedback input-impedance enhancement and a DC-servo loop; their simulated design reached 96.7 dB CMRR and 1.8 GΩ input impedance at 10 Hz [3]. Therefore, the design of modern chopper-stabilized AFEs is a system-level issue that includes noise, offset, input impedance and switching artifacts simultaneously.

3.2. Weak-inversion Biasing, Current Reuse and Voltage Scaling

A second family of techniques directly addresses power consumption. Lowering the supply voltage reduces power consumption at a constant current, and weak-inversion or subthreshold biasing can achieve a high transconductance-to-current ratio. Bai and Zhu used a 0.5 V supply, subthreshold input devices, capacitive coupling, transconductance boosting and chopping in a wireless biopotential instrumentation amplifier [7]. The entire front-end, including the DC-servo loop, drew 1.5 μA from 0.5 V and consumed approximately 0.75 μW, with 4.3 μVrms input-referred noise integrated from 0.5 Hz to 1 kHz and a CMRR of 98 dB [7]. The noise is higher than the sub-microvolt values of some microwatt designs, but the wide integration band and low supply must be considered before judging the result.

Current reuse increases efficiency by having the same bias current contribute to transconductance in multiple devices or stages. Song et al. combined current reuse with multiple supply voltages to optimize both current and voltage domains [6]. Kosari et al. used aggressive voltage scaling and weak-inversion techniques in a 0.5 V AFE that consumed only 68 nW, and allocated the largest share

of the power budget to the first low-noise stage because this stage accounts for most of the input noise [12]. This suggests a practical design rule: power need not be distributed equally among AFE stages. Later filter and gain stages can often use a smaller current because the first-stage gain reduces their noise contribution when referred to the system input.

Harpe et al. demonstrated extreme power reduction. Their 3 nW acquisition IC includes an amplifier, a 10-bit successive-approximation-register (SAR) ADC, a clock generator and bias circuitry, and successfully recorded ECG while powered by energy harvested from indoor light [11]. However, the reported total input noise was 27 μVrms. That operating point may be suitable for some detection tasks that require a relatively large signal amplitude, but its higher noise may obscure low-amplitude ECG features. The comparison shows the main result of this paper: extremely low power can limit the information that the system can obtain reliably.

3.3. Offset Rejection, Input Impedance and Common-Mode Robustness

Noise and power cannot be optimized independently of electrode offset and common-mode interference. Electrode polarization can cause a large DC offset and saturate a high-gain amplifier if this offset is amplified directly. Therefore, capacitive coupling is frequently used in wearable ECG AFEs to block DC and pass the desired AC biopotential signal to the amplifier. DC-servo loops can also be used to set the low-frequency corner and cancel residual offset [3,7]. These techniques introduce trade-offs in area, settling time, noise and loop stability.

A relatively high input impedance is also required for dry electrodes because their interface impedance can be large and variable. If the AFE input impedance is not much higher than the electrode impedance, the ECG signal can be attenuated and common-mode signals can convert to differential error. Ding et al. presented a wearable bioelectrical front-end that uses a shared DC-bias arrangement and a virtual right-leg drive to enhance practical CMRR without requiring extremely precise matching of peripheral components; the developed ECG system achieved 100 dB CMRR in their reported experiments [13]. Recently, integrated designs have employed positive feedback or carefully designed capacitive coupling to raise the input impedance to the gigaohm range [3,10].

These constraints explain why low amplifier noise alone cannot ensure reliable ECG acquisition. In practice, even an amplifier with low intrinsic noise may have poor recording performance if the system is saturated by electrode offset, converts common-mode interference into differential errors, or loads a high-impedance electrode. Therefore, a good AFE is a multi-objective design that needs to keep noise, power, input impedance, CMRR, offset tolerance and settling behavior within reasonable bounds simultaneously. Table 2 shows the main benefits, limitations and representative references of the techniques mentioned in this section.

Table 2. Comparison of Major Low-Frequency Noise and Power Techniques

Technique	Main benefit	Main cost / limitation	Representative sources
Chopper stabilization	Strong reduction of 1/f noise and offset	Ripple, spikes, switching artifacts, input-impedance challenges	[3,6,8,9]
Auto-zero / sampled correction	Cancels offset and low-frequency error	Aliasing and sampled kT/C-related noise; clocking required	[8]
Weak-inversion biasing	High transconductance efficiency at low current	Reduced speed/headroom and greater PVT sensitivity	[7,12]
Current reuse	More effective transconductance from a given current	Topology complexity and headroom constraints	[6]
Voltage scaling	Direct reduction of $P = VI$	Less signal swing and harder high-gain design	[7,11,12]
Capacitive coupling + DSL	Blocks electrode DC offset; sets low-frequency corner	Large effective time constants; settling/area concerns	[3,7,10]
Adaptive / programmable bias	Spend power only when needed	Control complexity and transient verification	[3,9,10]

4. Comparative Results and Discussion

4.1. Published Power-Noise Operating Points

Table 3 shows representative designs used in the quantitative comparison. The values are taken from the original papers or abstracts, and the authors' reported measurement bandwidths are preserved where available. The table intentionally includes both measured and simulated work because recent circuit research often presents post-layout simulation before silicon measurement; simulated entries are marked to distinguish them from measured hardware results. The designs also vary in whether power refers only to the amplifier, the full AFE, or a wider acquisition IC. These differences in reporting scope must be considered when interpreting the comparison.

Table 3. Representative low-power ECG/biopotential AFE results from the literature

Work	Supply / power	Input-referred noise	Other reported result	Status
Song et al., 2015 [6]	0.3/0.6/1.2 V; 1.56 µW system	0.34 µVrms (0.7–182 Hz)	NEF 1.74 core; PEF 1.41 system	Measured
Bai & Zhu, 2016 [7]	0.5 V; ~0.75 µW front end	4.3 µVrms (0.5 Hz–1 kHz)	98 dB CMRR	Measured
Harpe et al., 2016 [11]	0.6 V; 3 nW acquisition IC	27 µVrms	32 dB gain; 370 Hz BW; NEF 2.1 amplifier	Measured
Kosari et al., 2018 [12]	0.5 V; 68 nW AFE	2.8 µVrms (1.5–155 Hz)	31–52 dB gain; PEF 3.9	Measured
Yang et al., 2021 [9]	4 µW AFE	0.39 µVrms	NEF 2.4; prototype showed clear P wave	Measured
Han et al., 2023 [10]	1.2 V; 48 µW AFE	0.6 µV integrated	1.4 GΩ @ 50 Hz; 93 dB CMRR	Post-simulation
Sadeghi & Yavari, 2026 [3]	1.8 V; 2.44 µA (~4.39 µW)	Not stated in abstract	NEF 6.15; 96.7 dB CMRR; 1.8 GΩ @ 10 Hz	Simulation

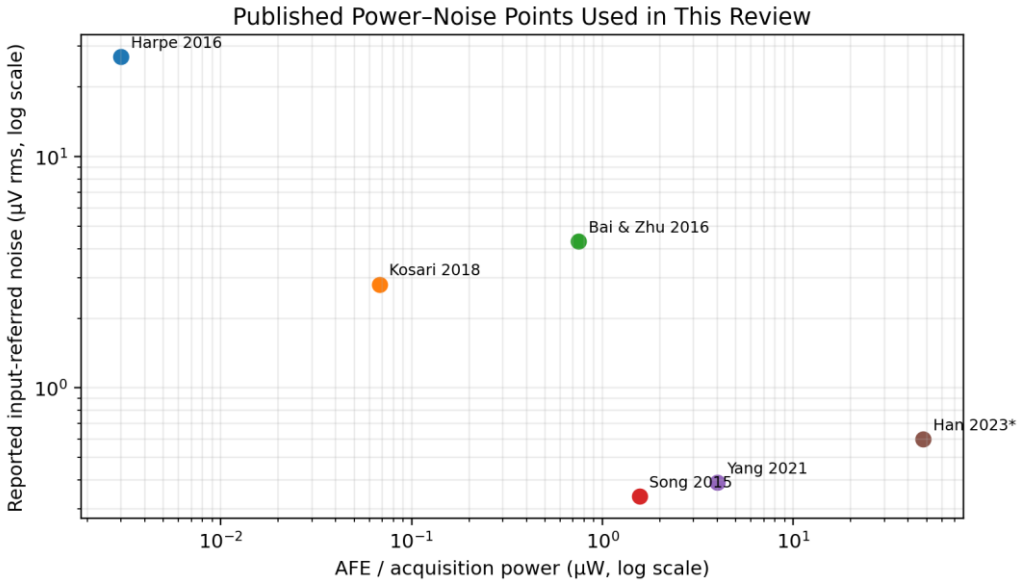

Fig. 2 Reported power versus integrated input-referred noise for six published designs [6,7,9-12]. (Picture credit: Original)

(Data from: Published results in Song et al. [6], Bai and Zhu [7], Yang et al. [9], Han et al. [10], Harpe et al. [11], and Kosari et al. [12].)

*Han et al.: post-simulation results. Integration bandwidths and system boundaries differ; the plot compares reported operating points and is not a strict benchmark.

The Harpe design [11] occupies the lowest-power operating point in Figure 2. It consumes several orders of magnitude less power than microwatt ECG front-ends but has higher input-referred noise, reflecting its different optimization goal. The circuit targets miniature, energy-limited sensor nodes, and the ADC and supporting circuits have been integrated into a 3 nW acquisition IC. For a system that needs to run on harvested indoor light, this trade-off is reasonable. However, for high-fidelity morphology, 27 µVrms is a relatively large proportion of the amplitude of small ECG features.

Kosari et al. report an intermediate operating point: 68 nW with 2.8 μVrms across 1.5–155 Hz [12]. Their work shows that careful weak-inversion design and low supply voltage can reduce power below 100 nW without accepting the tens-of-microvolts noise of the extreme 3 nW design. The architecture prioritizes the first stage in its power allocation; the first low-noise stage has a relatively large share of the power budget, and the following stages consume less. This is consistent with cascaded-noise analysis; the first stage has a larger impact on input-referred noise.

The Song and Yang designs occupy the lower-noise, higher-power region of the comparison. Both have microwatt-level power consumption and approximately 0.4 μVrms noise [6,9]. Song's work combines current reuse and chopper stabilization with efficient power management for multiple supply voltages, while Yang's design integrates chopping, passive filtering, digitally assisted offset cancellation, programmable gain, and an ADC with dynamic range scaling. The similar noise levels achieved by these different architectures suggest that sub-microvolt integrated noise benefits from coordinated noise-reduction and offset-control techniques as well as sufficient bias current. Switching artifacts, offset recovery, ADC interaction and electrode behavior all need to be handled.

The 4.3 μVrms noise reported by Bai and Zhu [7] was integrated over a wider band of 0.5 Hz–1 kHz. This wider bandwidth contributes to the higher integrated-noise value and illustrates why AFEs should not be ranked using a single noise number. Han et al. also reported 0.6 μV at 48 μW with high simulated input impedance and CMRR, but these are post-simulation results rather than silicon measurements [10]. Sadeghi and Yavari focus on a combination of high CMRR, high input impedance, DC-offset tolerance, programmable gain and chopper-spike suppression; their 2026 simulated result is about 4.39 μW but reports NEF rather than a directly comparable integrated-noise value in the abstract [3].

The comparison suggests a multi-objective trade-off, although the different test conditions prevent a formal Pareto ranking. Different designs suit different application requirements. A batteryless heart-rate sensor may consume tens of nanowatts and tolerate several microvolts of noise. An AFE intended to preserve P waves or other low-amplitude morphological features may consume a few microwatts to achieve sub-microvolt noise. Between the two, a practical AFE for long-term wearable monitoring may target sub-100 nW to low-microwatt power, a few microvolts or less of in-band input noise, high input impedance, and good CMRR. The specific target should be selected according to the purpose of the clinical or wellness application, not taken from the lowest number in the comparison table.

4.2. Design Implications for a Wearable ECG AFE

A practical design strategy follows from the comparison. First, limit the signal bandwidth to only that required by the application. An unnecessarily wide bandwidth increases integrated noise, and a larger current may be required to maintain gain and stability. Second, the first amplifier stage needs to have sufficient power to meet the noise requirement, because later stages cannot recover signal information already obscured by first-stage noise. Third, if a very low in-band noise is required by the application, then low-frequency flicker noise should be handled by chopping or another method, but the design must explicitly control switching ripple and input-impedance degradation [3,8].

Fourth, electrode DC offset and motion must be treated as primary design constraints. Capacitive coupling and a DC-servo loop can prevent saturation, but the corresponding high-pass corner and recovery time need to be verified. Fifth, programmable or adaptive bias is attractive for wearables because the circuit does not always need its maximum performance. The front end can remain in a low-current state during stable acquisition and temporarily increase the bias after a large motion artifact, electrode reconnection, or detected signal-quality degradation. Recent digitally assisted AFEs have shown that analog performance and digital control are increasingly co-designed rather than optimized separately [3,9,10].

Finally, evaluation should use more than NEF or power. A complete design report should specify at least the following: power supply voltage, integration bandwidth, input-referred noise, gain, input impedance at a particular frequency, CMRR at a particular frequency, electrode-offset tolerance, and

whether the results are from simulation or measurement. Without these data, an apparent efficiency improvement may simply reflect a narrower bandwidth or the exclusion of support circuitry from the power budget. Table 4 shows application-oriented recommendations based on this review. Figure 3 shows the above priorities in a workflow that starts with the ECG use case and then goes through performance goals, architecture selection, noise reduction, bias optimization and validation.

Table 4. Application-oriented design priorities derived from the literature comparison

Wearable use case	Primary priority	Reasonable design emphasis
Battery-less / energy-harvested sensing	Absolute power	Aggressive voltage scaling, weak inversion, narrow required bandwidth; accept higher noise if task allows
Long-term rhythm monitoring	Balanced power and noise	Sub-μW to low-μW AFE, strong offset handling, high input impedance, programmable gain
Morphology / visible P-wave monitoring	Very low in-band noise	Chopper stabilization, careful first-stage bias, ripple suppression, robust ADC interface
Dry-electrode daily activity	Input impedance and CMRR	GΩ-class input, mismatch tolerance, motion/offset recovery, common-mode suppression

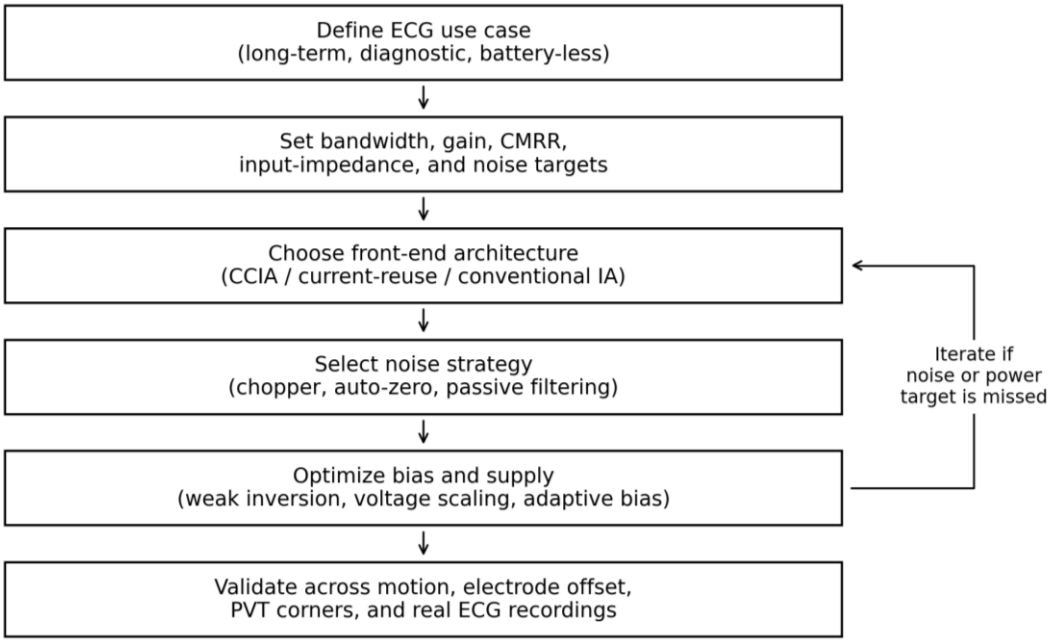

Fig. 3 Proposed application-first design framework for low-power wearable ECG AFEs, synthesized from [1,3,6,7,9-13]. (Picture credit: Original)

PVT: process, voltage and temperature. The framework is an original synthesis of the reviewed design priorities.

4.3. Limitations and Future Prospects

The main limitation of this study is the lack of standardized experimental conditions across the published AFE results. Input-referred noise values use different integration bands, and some papers report a complete AFE; others only report an amplifier core or a larger acquisition system. The designs use different process technologies and supply voltages, and some include an ADC or power-management circuit. A design with a wider bandwidth may appear noisier even if its noise spectral density is relatively low. A design whose reported power includes support circuitry may appear less efficient than one that reports only amplifier-core power. Therefore, the scatter plot cannot be regarded as a definitive ranking.

A second limitation is the discrepancy between simulation and silicon measurement. The Han 2023 and Sadeghi-Yavari 2026 results used in this review are simulation or post-simulation results [3,10], while the older Song, Bai, Harpe, Kosari, and Yang results include measured hardware [6,7,9,11,12]. Parasitic capacitance, device mismatch, electrode interface, clock feedthrough, package effects and

real motion can all degrade performance after fabrication. Future comparisons should distinguish pre-layout simulation, post-layout simulation, bench measurements and on-body tests as separate levels of evidence.

Third, circuit-level noise is only one type of degradation for wearable ECG signals. Motion artifacts and changes in electrode-skin impedance are common in actual recordings. Recent reviews of dynamic ECG noise suppression identify continuing difficulties in comparing algorithms across studies and datasets [5]. A very low-noise AFE cannot ensure a clean recording if the mechanical contact is unstable. Therefore, future wearable systems should integrate analog robustness, electrode design, signal-quality estimation, adaptive filtering and intelligent processing. The analog and digital subsystems should be designed together to meet a shared signal-quality goal.

Adaptive biasing is a promising direction. Instead of using an operational amplifier with a fixed current for the worst-case scenario, a low-current state can be employed during stable ECG acquisition, and then the current may be increased temporarily for faster recovery or lower noise. A second direction is digitally assisted analog design that uses digital calibration to correct offset, adjust gain, change bandwidth, or control chopping and bias. Yang et al. have already shown the advantages of PWM-based offset cancellation and an ADC with dynamic range scaling [9], and newer work continues to add programmable and recovery functions [3,10]. Event-driven operation may reduce average power if signal quality and recovery performance are maintained.

A third direction is improved management of chopping artifacts. The 2026 chopper-spike-filter method shows that the future of low-noise AFEs may involve additional circuits to mitigate the negative effects of noise reduction techniques [3]. A fourth priority is standardized reporting. Researchers should report the integrated noise along with bandwidth, spectral density at representative frequencies, total AFE power, amplifier-core power, CMRR frequency, input-impedance frequency, offset tolerance and measurement conditions. This would make NEF and PEF comparisons more meaningful and reduce the risk of comparing incompatible operating points.

Finally, the design goal will probably be more specific to an application. Future wearable ECG devices may range from unobtrusive energy-harvesting patches for simple event detection to more capable systems that preserve detailed morphology and perform local machine learning. These applications are likely to require different operational-amplifier architectures. Therefore, an important research direction is adaptive multi-objective optimization; energy, noise, dynamic range, input impedance, interference rejection, recovery time and computational requirements all need to be optimized simultaneously.

5. Conclusion

This paper investigates the noise-power trade-off in low-power operational-amplifier-based analog front-ends for wearable ECG monitoring. Across the reviewed studies, reducing power and reducing noise are related but conflicting objectives. Extreme nanowatt acquisition is possible, as shown by a 3 nW integrated system, but the reported system accepts significantly higher input-referred noise. Designs in the tens-of-nanowatts range can achieve ECG acquisition with a few microvolts of noise, and sub-microvolt noise generally occurs in microwatt-class systems that employ chopper stabilization, current reuse, careful first-stage biasing, and digitally assisted offset or ripple control. Chopping is effective in reducing low-frequency flicker noise, but it introduces switching artifacts and input-impedance problems that need to be solved at the system level. Based on the comparison, the power and noise values are only meaningful when bandwidth, CMRR, input impedance, offset tolerance and measurement conditions are also considered. Future wearable ECG systems should be optimized against application-specific requirements rather than a single metric. Designers should start with the required ECG information, prioritize the noise-critical first stage in the power budget, use adaptive or programmable operation when possible, and report standardized multi-metric results. This approach can extend wearable operating time while maintaining the signal fidelity required by the intended application.

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